1.  
\[ 13 + 10 = 001101 + 001010 = 010111 \]
\[ 15 + (-18) = 001111 + 101110 = 111101 \]
\[ 27 + (-6) = 011011 + 111010 = 010101 \]
\[ -6 + (-15) = 111010 + 110001 = 101011 \]
\[ 21 + (-21) = 010101 + 101011 = 000000 \]
\[ 31 + 12 = 011111 + 001100 = 101011 \]

The last value overflowed (43 can't be represented in a 2's complement 6-bit number).

2. Sum requires \( N + 1 \) bits, product requires \( N + M \) bits.

3. (a.) \[ t_{\text{setup}} = t_{pd,CL1} + t_{s,R1} = 9 \] (CL1 delays the arrival of stable IN at R1)
\[ t_{pd} = t_{pd,R2} = 5 \] (OUT comes from R2)
\[ t_{clk} > t_{pd,R1} + t_{pd,CL2} + t_{\text{setup,R2}} = 15 \]

(b.) \[ t_{\text{setup}} = t_{pd,CL1} + t_{s,R1} - \delta_1 = 7 - \delta_1 \]

(R1 is clocked after the rising edge of CLK, so IN can become stable a little later and still meet the setup time of R1)

\[ t_{pd} = \delta_2 + t_{pd,r2} = \delta_2 + 5 \]

(R2 is clocked after the rising edge of CLK, so its output appears a little later than in part A).

(c.) \[ t_{clk} + \delta_2 > \delta_1 + t_{pd,R1} + t_{pd,CL2} + t_{\text{setup,R2}} \text{ or } t_{clk} > (\delta_1 - \delta_2) + 15 \]

If \( \delta_1 > \delta_2 \) and R1 is clocked before R2, tclk must be longer to account for the smaller interval between clocking the two registers. If \( \delta_1 < \delta_2 \), R1 is clocked before R2, adding a bit to the interval between the two regs and tclk can be made smaller.

4. (a.) Latency of longest path = 2 + 3 + 4 = 9

(b.) When pipelining, we always add a register to the output, but a 1-stage pipeline makes no change in the latency or throughput. Adding another register to the
output and looking for a retiming contour that minimizes the number of new registers, we find the contour passes through the circuit just before the "4" module. For this 2-stage pipeline:

\[ t_{\text{clk}} = 5, \ L = 10, \ T = 1/5. \]

It requires 3 registers.

(c.) We can make a 3-stage pipeline with \( t_{\text{clk}} = 4, \ L = 12, \ T = 1/4 \), but additional registers won't improve \( t_{\text{clk}} \) since that's set by the stage containing the "4" module. So the maximum throughput is 1/4.

(d.) The lower bound on the latency is set by a 1-stage pipeline: \( L = 9 \). For this circuit, any additional pipelining will result in latency that's larger. In general the latency stays the same or gets worse with pipelining; it's never improved.