Computer Architecture and Performance Engineering

Saman Amarasinghe
Fall 2011
Outline

Overview of Computer Architecture
Profiling a Program
Set of Example Programs
Computer Architecture Overview

Instructions
Memory System
Processor Bus and IO Subsystem
Disk System
GPU and Graphics System
Network

courtesy of Intel Corp.
Instructions

Memory System

courtesy of Intel Corp.
Instruction Execution

Instruction #  

Instruction i
Instruction i+1
Instruction i+2
Instruction i+3
Instruction i+4

Cycles

1 2 3 4 5 6 7 8 9 10
Instruction Execution

IF: Instruction fetch  ID: Instruction decode
EX: Execution          MEM: Memory access
WB: Write back

Cycles

Instruction #  1  2  3  4  5  6  7  8  9  10

Instruction i  IF  ID  EX  MEM  WB
Instruction i+1 IF  ID  EX  MEM  WB
Instruction i+2 IF  ID  EX  MEM  WB
Instruction i+3 IF  ID  EX  MEM  WB
Instruction i+4 IF  ID  EX  MEM  WB
Pipelining Execution

IF: Instruction fetch
ID : Instruction decode
EX : Execution
MEM: Memory access
WB : Write back

Cycles
Limits to pipelining

**Hazards** prevent next instruction from executing during its designated clock cycle

- **Structural hazards**: attempt to use the same hardware to do two different things at once
- **Data hazards**: Instruction depends on result of prior instruction still in the pipeline
- **Control hazards**: Caused by delay between the fetching of instructions and decisions about changes in control flow (branches and jumps).
Data Hazards: True Dependence

Instr$_j$ is **data dependent** (aka **true dependence**) on Instr$_i$:

\[
\text{addl } \text{rbx, rax} \leftarrow J: \text{subl } \text{rax,rcx}
\]

If two instructions are data dependent, they cannot execute simultaneously, be completely overlapped or execute in out-of-order.

If data dependence caused a hazard in pipeline, called a **Read After Write (RAW)** hazard.
Benefits of Unrolling

```c
int A[1000000];
int B[1000000];
test()
{
    int i;
    for(i=0; i <1000000; i++)
}
```

For(i=0; i<N; i += 4) {
    A[i+1] = A[i+1] + 1
}
```asm
xorl %edx, %edx
.B1.2:
    movl B(%rdi), %eax
    movl 4+B(%rdi), %edx
    movl 8+B(%rdi), %ecx
    movl 12+B(%rdi), %esi
    addl %eax, A(%rdi)
    addl %edx, 4+A(%rdi)
    addl %ecx, 8+A(%rdi)
    addl %esi, 12+A(%rdi)
    addq $16, %rdi
    cmpq $4000000, %rdi
    jl ..B1.2
.B1.3:
    ret
```
Name dependence: when 2 instructions use same register or memory location, called a name, but no flow of data between the instructions associated with that name; 2 versions of name dependence

Instr₁ writes operand before Instr₂ reads it

\[ \text{subl } rax, rbx \]
\[ \text{addl } rcx, rax \]

Called an “anti-dependence” by compiler writers. This results from reuse of the name “rax”

If anti-dependence caused a hazard in the pipeline, called a Write After Read (WAR) hazard
Name Dependence #2: Output dependence

Instr\(I\) writes operand before Instr\(J\) writes it.

\[
\begin{align*}
&\text{subl rcx, rax} \\
&\text{addl rbx, rax}
\end{align*}
\]

Called an “output dependence” by compiler writers. This also results from the reuse of name “rax”

If anti-dependence caused a hazard in the pipeline, called a **Write After Write (WAW) hazard**

Instructions involved in a name dependence can execute simultaneously if name used in instructions is changed so instructions do not conflict

- Register renaming resolves name dependence for registers
- Renaming can be done either by compiler or by HW
Control Hazards

Every instruction is control dependent on some set of branches, and, in general, these control dependencies must be preserved to preserve program order

```c
if p1 {
    S1;
}
if p2 {
    S2;
}
```

*S1 is control dependent on p1, and S2 is control dependent on p2 but not on p1.*

Control dependence need not be preserved

➢ willing to execute instructions that should not have been executed, thereby violating the control dependences, if can do so without affecting correctness of the program

Speculative Execution
Intel® Nehalem™ Microarchitecture – Pipelining

20-24 stage Pipeline
courtesy of Intel Corp.
Superscalar Execution

2-issue super-scalar machine
ILP and Data Hazards

**Finds Instruction Level Parallelism**
- Multiple instructions issued in parallel

**HW/SW must preserve program order:**
order instructions would execute in if executed sequentially as determined by original source program
- Dependences are a property of programs

**Importance of the data dependencies**
- 1) indicates the possibility of a hazard
- 2) determines order in which results must be calculated
- 3) sets an upper bound on how much parallelism can possibly be exploited

**Goal:** exploit parallelism by preserving program order only where it affects the outcome of the program
Multimedia Instructions

SIMD:

- In computing, **SIMD** (Single Instruction, Multiple Data) is a technique employed to achieve data level parallelism, as in a vector or array processor.

- Intel calls the latest version **SSE**
Multimedia Instructions

Packed data type
➢ Separate register file

Single Instruction on Multiple Data (SIMD)

Figure 4: Packed Operation
courtesy of x86.org
Multimedia Instructions

Vectorization Converts Loops

for (l=0; l<=MAX; l++)
c[l]=a[l]+b[l];


int A[1000000];
int B[1000000];
test()
{
  int i;
  for(i=0; i<1000000; i++)
}

xorl   %edx, %edx

..B1.2:
  movdqa A(%rax), %xmm0
  paddd B(%rax), %xmm0
  movdqa 16+A(%rax), %xmm1
  paddd 16+B(%rax), %xmm1
  movdqa 32+A(%rax), %xmm2
  paddd 32+B(%rax), %xmm2
  movdqa 48+A(%rax), %xmm3
  paddd 48+B(%rax), %xmm3
  movdqa 64+A(%rax), %xmm4
  paddd 64+B(%rax), %xmm4
  movdqa 80+A(%rax), %xmm5
  paddd 80+B(%rax), %xmm5
  movdqa 96+A(%rax), %xmm6
  paddd 96+B(%rax), %xmm6
  movdqa 112+A(%rax), %xmm7
  paddd 112+B(%rax), %xmm7
  movdqa %xmm0, A(%rax)
  movdqa %xmm1, 16+A(%rax)
  movdqa %xmm2, 32+A(%rax)
  movdqa %xmm3, 48+A(%rax)
  movdqa %xmm4, 64+A(%rax)
  movdqa %xmm5, 80+A(%rax)
  movdqa %xmm6, 96+A(%rax)
  movdqa %xmm7, 112+A(%rax)
  addq $128, %rax
  cmpq $4000000, %rax
  jl ..B1.2

..B1.3:
ret
Intel® Nehalem™ Microarchitecture – Superscalar Execution

Can execute 6 Ops per cycle

3 Memory Operations
- Load
- Store address
- Store data

3 Computational Operations
Out of Order Execution

Issue varying numbers of instructions per clock

- dynamically scheduled
  - Extracting ILP by examining 100’s of instructions
  - Scheduling them in parallel as operands become available
  - Rename registers to eliminate anti and dependences
  - out-of-order execution
  - Speculative execution
Out of order Execution

\[ A[I] = B[I] \]
\[ X[I] = Y[I] \]

\( I \) in %rd
\( B \) in %rsi
\( A \) in %rdi
\( Y \) in %r8
\( X \) in %rcx

\texttt{movl} (\%rsi, \%rdx, 4), \%eax
\texttt{movl} \%eax, (\%rdi, \%rdx, 4)
\texttt{movl} (\%r8, \%rdx, 4), \%eax
\texttt{movl} \%eax, (\%rcx, \%rdx, 4)
Out of order Execution

\[ A[I] = B[I] \]
\[ X[I] = Y[I] \]

\( I \) in \%rd
\( B \) in \%rsi
\( A \) in \%rdi
\( Y \) in \%r8
\( X \) in \%rcx

\[
\begin{align*}
\text{movl} & \quad (%rsi, %rdx, 4), %eax \\
\text{movl} & \quad %eax, (%rdi, %rdx, 4) \\
\text{movl} & \quad (%r8, %rdx, 4), %eax \\
\text{movl} & \quad %eax, (%rcx, %rdx, 4)
\end{align*}
\]
Out of order Execution

\[ A[I] = B[I] \]
\[ X[I] = Y[I] \]

Register Renaming

I in %rd
B in %rsi
A in %rdi
Y in %r8
X in %rcx

\[
\begin{align*}
\text{movl} &\ (\%rsi, \%rdx, 4), \%eax \\
\text{movl} &\ %eax, (\%rdi, \%rdx, 4) \\
\text{movl} &\ (\%r8, \%rdx, 4), \%ebx \\
\text{movl} &\ %ebx, (\%rcx, \%rdx, 4)
\end{align*}
\]
Out of order Execution

$A[I] = B[I]$
$X[I] = Y[I]$

$I$ in %rd
$B$ in %rsi
$A$ in %rdi
$Y$ in %r8
$X$ in %rcx

<table>
<thead>
<tr>
<th>movl (%rsi, %rdx, 4), %eax</th>
<th>movl (%r8, %rdx, 4), %ebx</th>
</tr>
</thead>
<tbody>
<tr>
<td>movl %eax, (%rdi, %rdx, 4)</td>
<td>movl %ebx, (%rcx, %rdx, 4)</td>
</tr>
</tbody>
</table>

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Out of order Execution

A[I] = B[I]
X[I] = Y[I]

I in %rd
B in %rsi
A in %rdi
Y in %r8
X in %rcx

B[I] is a cache miss

<table>
<thead>
<tr>
<th>movl (%rsi, %rdx, 4), %eax</th>
<th>movl (%r8, %rdx, 4), %ebx</th>
</tr>
</thead>
<tbody>
<tr>
<td>movl %ebx, (%rcx, %rdx, 4)</td>
<td></td>
</tr>
</tbody>
</table>

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Out of order Execution

A[I] = B[I]
X[I] = Y[I]

Assume A[I] == Y[I]

l in %rd
B in %rsi
A in %rdi
Y in %r8
X in %rcx

\[
\begin{align*}
\text{movl} & (\%rsi, \%rdx, 4), \%eax \\
\text{movl} & (\%r8, \%rdx, 4), \%ebx \\
\text{movl} & \%ebx, (\%rcx, \%rdx, 4) \\
\end{align*}
\]
Out of order Execution

A[I] = B[I]
X[I] = Y[I]

I in %rd
B in %rsi
A in %rdi
Y in %r8
X in %rcx

Assume A[I] == Y[I]
Write buffer
either delay
or predict and squash

movl (\%rsi, \%rdx, 4), \%eax
movl \%eax, (\%rdi, \%rdx, 4)
movl (\%r8, \%rdx, 4), \%ebx
movl \%ebx, (\%rcx, \%rdx, 4)
Speculation

Different predictors
- Branch Prediction
- Value Prediction
- Prefetching (memory access pattern prediction)

**Greater ILP**: Overcome control dependence by hardware speculating on outcome of branches and executing program as if guesses were correct

- **Speculation** ⇒ fetch, issue, and execute instructions as if branch predictions were always correct
- **Dynamic scheduling** ⇒ only fetches and issues instructions

Essentially a **data flow execution model**: Operations execute as soon as their operands are available
Intel® Nehalem™ Microarchitecture - Out of Order Execution

20 to 24 stage Pipeline

6 micro-ops issued at a time

128 micro-ops waiting to be executed

courtesy of Intel Corp.
Branch Prediction and Speculative Execution

Instruction # | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10
---|---|---|---|---|---|---|---|---|---|---
Instruction i (branch) | IF | ID | EX | MEM | WB | WB | WB | WB | WB | WB
Instruction i+1 | IF | ID | EX | MEM | WB | WB | WB | WB | WB | WB
Instruction i+2 | IF | ID | EX | MEM | WB | WB | WB | WB | WB | WB
Instruction i+3 | IF | ID | EX | MEM | WB | WB | WB | WB | WB | WB
Instruction i+4 | IF | ID | EX | MEM | WB | WB | WB | WB | WB | WB
Instruction i+5 | IF | ID | EX | MEM | WB | WB | WB | WB | WB | WB

Branch target decided
Branch Prediction and Speculative Execution

Instruction # 1 2 3 4 5 6 7 8 9 10

Instruction i (branch) [IF] [ID] [EX] [MEM] [WB]

Branch target decided

Instruction i+1

Cycles

stall
stall
stall
stall
stall
Branch Prediction and Speculative Execution

**Build a predictor to figure out which direction branch is going**
- Today we have complex predictors with 99+% accuracy
- Even predict the address in indirect branches / returns

**Fetch and speculatively execute from the predicted address**
- No pipeline stalls

**When the branch is finally decided, the speculative execution is confirmed or squashed**
Complex predictor
Multiple predictors
➢ Use branch history
➢ Different algorithms
➢ Vote at the end
Indirect address predictor
Return address predictor

Nehalem is even more complicated!
Memory System

The Principle of Locality:

- Program access a relatively small portion of the address space at any instant of time.

Two Different Types of Locality:

- **Temporal Locality** (Locality in Time): If an item is referenced, it will tend to be referenced again soon (e.g., loops, reuse)
- **Spatial Locality** (Locality in Space): If an item is referenced, items whose addresses are close by tend to be referenced soon (e.g., straight-line code, array access)

Last 30 years, HW relied on locality for memory perf.
Levels of the Memory Hierarchy

- **CPU Registers**
  - 100s Bytes
  - 300 – 500 ps (0.3-0.5 ns)

- **L1 and L2 Cache**
  - 10s-100s K Bytes
  - ~1 ns - ~10 ns
  - $1000s/ GByte

- **Main Memory**
  - G Bytes
  - 80ns- 200ns
  - ~ $100/ GByte

- **Disk**
  - 10s T Bytes, 10 ms
  - (10,000,000 ns)
  - ~ $1 / GByte

- **Tape**
  - infinite
  - sec-min
  - ~$1 / GByte

**Capacity**
- CPU Registers: 100s Bytes
- L1 and L2 Cache: 10s-100s K Bytes
- Main Memory: G Bytes
- Disk: 10s T Bytes
- Tape: infinite

**Access Time**
- CPU Registers: 300 – 500 ps
- L1 and L2 Cache: ~1 ns - ~10 ns
- Main Memory: 80ns- 200ns
- Disk: 10 ms
- Tape: infinite

**Cost**
- CPU Registers: ~ $1000s/ GByte
- L1 and L2 Cache: $1000s/ GByte
- Main Memory: ~ $100/ GByte
- Disk: ~ $1 / GByte
- Tape: ~$1 / GByte
Cache Issues

**Cold Miss**
- The first time the data is available
- Prefetching may be able to reduce the cost

**Capacity Miss**
- The previous access has been evicted because too much data touched in between
- “Working Set” too large
- Reorganize the data access so reuse occurs before getting evicted.
- Prefetch otherwise

**Conflict Miss**
- Multiple data items mapped to the same location. Evicted even before cache is full
- Rearrange data and/or pad arrays

**True Sharing Miss**
- Thread in another processor wanted the data, it got moved to the other cache
- Minimize sharing/locks

**False Sharing Miss**
- Other processor used different data in the same cache line. So the line got moved
- Pad data and make sure structures such as locks don’t get into the same cache line
Intel® Nehalem™ Microarchitecture – Memory Sub-system

Intel 6 Core Processor

<table>
<thead>
<tr>
<th></th>
<th>L1 Data Cache</th>
<th>L1 Instruction Cache</th>
<th>L2 Cache</th>
<th>L3 Cache</th>
<th>Main Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size</td>
<td>32 KB</td>
<td>32 KB</td>
<td>256 KB</td>
<td>12 MB</td>
<td>64 bytes</td>
</tr>
<tr>
<td>Line Size</td>
<td>64 bytes</td>
<td>64 bytes</td>
<td>64 bytes</td>
<td>64 bytes</td>
<td>64 bytes</td>
</tr>
<tr>
<td>Latency</td>
<td>4 ns</td>
<td>4 ns</td>
<td>10 ns</td>
<td>50 ns</td>
<td>75 ns</td>
</tr>
<tr>
<td>Associativity</td>
<td>8-way</td>
<td>4-way</td>
<td>8-way</td>
<td>16-way</td>
<td></td>
</tr>
</tbody>
</table>
Memory Consistency

\[ A[I] = B[I] \]
\[ X[I] = Y[I] \]

I in %rd
B in %rsi
A in %rdi
Y in %r8
X in %rcx

\[
\text{movl} \enspace (%rsi, %rdx, 4), \%eax
\]

\[
\text{movl} \enspace \%eax, (%rdi, %rdx, 4)
\]

\[
\text{movl} \enspace (%r8, %rdx, 4), \%ebx
\]

\[
\text{movl} \enspace \%ebx, (%rcx, %rdx, 4)
\]

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Memory Consistency

\( A[I] = B[I] \)
\( X[I] = Y[I] \)

\( I \) in \%rd
\( B \) in \%rsi
\( A \) in \%rdi
\( Y \) in \%r8
\( X \) in \%rcx

What happens if another core is looking?
Memory Consistency

A[i] = .... while(!done);
done = 1

B = A[i]
Memory Consistency

\[ A[i] = \ldots \]
\[ \text{done} = 1 \]

while(!done);
\[ B = A[i] \]
Memory Consistency

A[i] = …. 
done = 1

while(!done);
B = A[i]

wr A[i]

rd done

rd done

rd done

rd A[i]
Memory Consistency

• Reordering of reads and writes in OOO can create an inconsistent view from the outside.

• If it matter to outside make sure that all the memory references are done before the communication is initiated.

• Memory fence instructions
  • Pros: get rid of the inconsistency
  • Cons: expensive

A[i] = ....
Mem fence while(!done);
B = A[i]
done = 1
Outline

Overview of Computer Architecture

Profileing a Program

Set of Example Programs
Performance Analyzer

Helps you identify and characterize performance issues by:

• Collecting performance data from the system running your application.

• Organizing and displaying the data in a variety of interactive views, from system-wide down to source code or processor instruction perspective.

• Identifying potential performance issues and suggesting improvements.

Example: Intel Vtune, gprof, oprofile, perf
What Is a Hotspot?

Where in an application or system there is a significant amount of activity

- Where = address in memory
  => OS process
  => OS thread
  => executable file or module
  => user function (requires symbols)
  => line of source code (requires symbols with line numbers) or assembly instruction

- Significant = activity that occurs infrequently probably does not have much impact on system performance

- Activity = time spent or other internal processor event
  - Examples of other events: Cache misses, branch mispredictions, floating-point instructions retired, partial register stalls, and so on.
Two Ways to Track Location

**Problem:** I need to know where you spend most of your time.

**Statistical Solution:** I call you on your cellular phone every 30 minutes and ask you to report your location. Then I plot the data as a histogram.

**Instrumentation Solution:** I install a special phone booth at the entrance of every site you plan to visit. As you enter or exit every site, you first go into the booth, call the operator to get the exact time, and then call me and tell me where you are and when you got there.
Sampling Collector

Periodically interrupt the processor to obtain the execution context

- Time-based sampling (TBS) is triggered by:
  - Operating system timer services.
  - Every $n$ processor clockticks.

- Event-based sampling (EBS) is triggered by processor event counter overflow.
  - These events are processor-specific, like L2 cache misses, branch mispredictions, floating-point instructions retired, and so on.
The Statistical Solution: Advantages

No Installation Required

- No need to install a phone everywhere you want a man in the field to make a report.

Wide Coverage

- Assuming all his territory has cellular coverage, you can track him wherever he goes.

Low Overhead

- Answering his cellular telephone once in a while, reporting his location, and returning to other tasks do not take much of his time.
The Statistical Solution:

Disadvantages

**Approximate Precision:**
- A number of factors can influence exactly how long he takes to answer the phone.

**Limited Report:**
- Insufficient time to find out how he got to where he is or where he has been since you last called him.

---

**Statistical Significance:** There are some places you might not locate him, if he does not go there often or he does not stay very long. Does that really matter?
The Instrumentation Solution: Advantages

Perfect Accuracy

- I know where you were immediately before and after your visit to each customer.
- I can calculate how much time you spent at each customer site.
- I know how many times you visited each customer site.
The Instrumentation Solution: Disadvantages

**Low Granularity**
- Too coarse; the site is the site.

**High Overhead**
- You spend valuable time going to phone booths, calling operators, and calling me.

**High Touch**
- I have to build all those phone booths, which expands the space in each site you visit.
Events

Intel provide 100’s of types of events

- Can be very confusing (ex: “number of bogus branches”)
- Some useful event categories
  - Total instruction count and mix
  - Branch events
  - Load/store events
  - L1/L2 cache events
  - Prefetching events
  - TLB events
  - Multicore events
Use Event Ratios

In isolation, events may not tell you much.

Event ratios are dynamically calculated values based on events that make up the formula.

- Cycles per instruction (CPI) consists of clockticks and instructions retired.

There are a wide variety of predefined event ratios.
Outline

Overview of Computer Architecture
Profiling a Program

Set of Example Programs
#define MAXA 10000
int maxa_half = MAXA/2;
int32_t A[MAXA];

// [0, 1, 2, 3, 4, ...]
int32_t incA[MAXA];

// [0..MAXA-1 randomly]
int32_t rndA[MAXA];
multiple passes over data

for(j=0; j<MAXA; j++)

..B3.3:
    incl (%rax)
    addq $4, %rax
    cmpq %rdx, %rax
    jl ..B3.3
Assembly listings

test div by 4

for(j=0; j<MAXA; j++) {
  if((j & 0x03) == 0)
}

xorl %edx, %edx

..B2.2:
testb $3, %dl
  jne ..B2.4

..B2.3:
  movslq %edx, %rax
  incl A(%rax,4)

..B2.4:
  incl %edx
  cmpl $10000, %edx
  jl ..B2.2

test incA[i] < maxa_half

for(j=0; j<MAXA; j++) {
  if(incA[j] < maxa_half)
}

movslq maxa_half(%rip), %rdx
xorl %ecx, %ecx
xorl %eax, %eax

..B1.2:
  cmpq incA(%rcx,8), %rdx
  jle ..B1.4

..B1.3:
  incl A(%rax)

..B1.4:
  addq $4, %rax
  addq $1, %rcx
  cmpq $10000, %rcx
  jl ..B1.2
## Results

<table>
<thead>
<tr>
<th>Test Condition</th>
<th>Runtime (ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>multi pass over</td>
<td>1.00</td>
</tr>
<tr>
<td>test j &lt; maxa_half</td>
<td>1.26</td>
</tr>
<tr>
<td>test div by 4</td>
<td>2.21</td>
</tr>
<tr>
<td>test incA[i] &lt; maxa_half</td>
<td>1.33</td>
</tr>
<tr>
<td>test rndA[i] &lt; maxa_half</td>
<td>6.80</td>
</tr>
</tbody>
</table>
## INST RETIRED.ANY

Instructions retired.

This event counts the number of instructions that retire execution. For instructions that consist of multiple micro-ops, this event counts the retirement of the last micro-op of the instruction. The counter continues counting during hardware interrupts, traps, and inside interrupt handlers.

<table>
<thead>
<tr>
<th>multi pass over</th>
<th>1.00</th>
<th>1.00</th>
</tr>
</thead>
<tbody>
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<td>test j &lt; maxa_half</td>
<td>1.26</td>
<td>1.50</td>
</tr>
<tr>
<td>test div by 4</td>
<td>2.21</td>
<td>1.37</td>
</tr>
<tr>
<td>test incA[i] &lt; maxa_half</td>
<td>1.33</td>
<td>1.63</td>
</tr>
<tr>
<td>test rndA[i] &lt; maxa_half</td>
<td>6.80</td>
<td>1.63</td>
</tr>
</tbody>
</table>

**RESULTS**

<table>
<thead>
<tr>
<th>Runtime (ms)</th>
<th>INST RETIRED.ANY</th>
</tr>
</thead>
<tbody>
<tr>
<td>INST RETIRED.ANY events</td>
<td></td>
</tr>
<tr>
<td>INST RETIRED.LOADS</td>
<td></td>
</tr>
<tr>
<td>BR INST RETIRED.ANY</td>
<td></td>
</tr>
<tr>
<td>Inst Retired (ANY - LOAD - BR)</td>
<td></td>
</tr>
<tr>
<td>Clocks per Instructions Retired</td>
<td></td>
</tr>
<tr>
<td>CPI</td>
<td></td>
</tr>
<tr>
<td>CPI*Tot Instructions</td>
<td></td>
</tr>
<tr>
<td>BR INST RETIRED.MIS PRED %</td>
<td></td>
</tr>
<tr>
<td>&quot;Instructions wasted&quot; of mispredicted branches</td>
<td></td>
</tr>
<tr>
<td>Total &quot;Cost&quot;</td>
<td></td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th>multi pass over</th>
<th>Runtime (ms)</th>
<th>INST_RETIRED.ANY events</th>
<th>INST_RETIRED.LODS events</th>
<th>BR_INST_RETIRED.ANY events</th>
<th>Inst Retired (ANY - LOAD - BR)</th>
</tr>
</thead>
<tbody>
<tr>
<td>test j &lt; maxa_half</td>
<td>1.26</td>
<td>1.50</td>
<td>0.50</td>
<td>1.99</td>
<td>1.75</td>
</tr>
<tr>
<td>test div by 4</td>
<td>2.21</td>
<td>1.37</td>
<td>0.25</td>
<td>1.99</td>
<td>1.62</td>
</tr>
<tr>
<td>test incA[i] &lt; maxa_half</td>
<td>1.33</td>
<td>1.63</td>
<td>1.50</td>
<td>2.00</td>
<td>1.50</td>
</tr>
<tr>
<td>test rndA[i] &lt; maxa_half</td>
<td>6.80</td>
<td>1.63</td>
<td>1.50</td>
<td>1.99</td>
<td>1.50</td>
</tr>
</tbody>
</table>

**INST_RETIRED.LODS**  Instructions retired, contain a load

**INST_RETIRED.STORE**  Instructions retired, contain a store

**BR_INST_RETIRED.ANY**  Number of branch instructions retired
<table>
<thead>
<tr>
<th>multi pass over</th>
<th>1.00</th>
<th>1.00</th>
<th>1.00</th>
<th>1.00</th>
</tr>
</thead>
<tbody>
<tr>
<td>test j &lt; maxa_half</td>
<td>1.26</td>
<td>1.50</td>
<td>0.84</td>
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</tr>
<tr>
<td>test div by 4</td>
<td>2.21</td>
<td>1.37</td>
<td>1.60</td>
<td>2.19</td>
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<tr>
<td>test incA[i] &lt; maxa_half</td>
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<td>1.63</td>
<td>0.82</td>
<td>1.33</td>
</tr>
<tr>
<td>test rndA[i] &lt; maxa_half</td>
<td>6.80</td>
<td>1.63</td>
<td>4.17</td>
<td>6.78</td>
</tr>
</tbody>
</table>

**CPI**

CPU_CLK_UNHALTED.CORE / INST_RETIRED.ANY

High CPI indicates that instructions require more cycles to execute than they should. In this case there may be opportunities to modify your code to improve the efficiency with which instructions are executed within the processor. CPI can get as low as 0.25 cycles per instructions.
results

<table>
<thead>
<tr>
<th></th>
<th>Runtime (ms)</th>
<th>BR_INST_RETIRED.MISPRED %</th>
</tr>
</thead>
<tbody>
<tr>
<td>multi pass over</td>
<td>1.00</td>
<td>1.00</td>
</tr>
<tr>
<td>test j &lt; maxa_half</td>
<td>1.26</td>
<td>2.50</td>
</tr>
<tr>
<td>test div by 4</td>
<td>2.21</td>
<td>400.00</td>
</tr>
<tr>
<td>test incA[i] &lt; maxa_half</td>
<td>1.33</td>
<td>2.00</td>
</tr>
<tr>
<td>test rndA[i] &lt; maxa_half</td>
<td>6.80</td>
<td>2134.00</td>
</tr>
</tbody>
</table>

**BR_INST RETIRED.MISPRED**

This event counts the number of retired branch instructions that were mispredicted by the processor. A branch misprediction occurs when the processor predicts that the branch would be taken, but it is not, or vice-versa. ....
### Results

<table>
<thead>
<tr>
<th></th>
<th>Runtime (ms)</th>
<th>INST_RETIRED.ANY events</th>
<th>BR_INST_RETIRED.MIS PRED %</th>
<th>&quot;Instructions wasted&quot; of mispredicted branches</th>
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<tbody>
<tr>
<td>Multi pass over</td>
<td>1.00</td>
<td>1.00</td>
<td>1.00</td>
<td>1.00</td>
<td>1.00</td>
</tr>
<tr>
<td>Test j &lt; maxa_half</td>
<td>1.26</td>
<td>1.50</td>
<td>2.50</td>
<td>4.97</td>
<td>1.50</td>
</tr>
<tr>
<td>Test div by 4</td>
<td>2.21</td>
<td>1.37</td>
<td>400.00</td>
<td>797.51</td>
<td>2.21</td>
</tr>
<tr>
<td>Test incA[i] &lt; maxa_half</td>
<td>1.33</td>
<td>1.63</td>
<td>2.00</td>
<td>3.99</td>
<td>1.63</td>
</tr>
<tr>
<td>Test rndA[i] &lt; maxa_half</td>
<td>6.80</td>
<td>1.63</td>
<td>2134.00</td>
<td>4254.69</td>
<td>6.10</td>
</tr>
</tbody>
</table>

Assume the cost of a mispredicted branch is 21 “instructions wasted”

- Number 21 got the closest answer