yesterday we discussed the behavior of MOSFET devices in subthreshold regime:

\[ I_{D_{st}} = I_{S_{st}} \cdot e^{\frac{q(V_{GS}-V_{T})}{nKT}} \left(1 - e^{-\frac{qV_{DS}}{nKT}}\right) \]

If we plot \( \log|I_{D_{st}}| \) vs \( V_{GS} \),

(for \( V_{GS} \gg \frac{kT}{q} \), \( I_{D_{st}} \approx I_{S_{st}} \cdot e^{\frac{q(V_{GS}-V_{T})}{nKT}} \))

This behavior is very much similar to the behavior of BJT device,

\[ i_c = I_S e^{\frac{qV_{BE}}{nKT}} \]
\[ i_B = \frac{I_S}{\beta_F} e^{\frac{qV_{BE}}{nKT}} \]

Today we will look carefully at why it is like this.

1. First, what is this "\( n \)"? (ideally, we would want \( n \approx 1 \))

consider the potential distribution \( \phi(x) \) with a specific \( V_{GS} \) applied: \( (V_{GS} < V_T) \)

\[ V_{GS} + \phi_B = V_{ox} + V_B \]

\[ \phi_B = V_{FB}, \quad V_B = \phi(x_0) - \phi_p \]

\[ V_{ox} = E_{ox} \cdot t_{ox} = t_{ox} \cdot \frac{Q_g}{E_{ox}} = t_{ox} \cdot \frac{E_{NA} \cdot x_D}{E_{ox}} \]

\[ \frac{E_{NA}}{2E_{Si}} \cdot x_D^2 = \phi(0) - \phi_p \Rightarrow x_D = \sqrt{\frac{2E_{Si} \cdot (\phi(0) - \phi_p)}{E_{NA}}} \]

\[ V_{GS} = V_{FB} + (\phi(0) - \phi_p) + \frac{1}{C_{ox}} \sqrt{2E_{Si} E_{NA} \cdot (\phi(0) - \phi_p)} \]

Now if we ask the question: in order to shift \( \phi(0) \), say by 10mV, how much should \( V_{GS} \) move?
\[ \Delta V_{GS} = \frac{dV_{GS}}{d\phi(0)} \cdot \Delta \phi(0). \]

Define \( n = \frac{dV_{GS}}{d\phi(0)} = 1 + \frac{1}{2C_{ox}} \sqrt{\frac{2\varepsilon_s N_A}{\Phi(0) - \Phi_D}} = 1 + \frac{C_{pp}}{C_{ox}}, \)

where \( C_{pp} = \frac{\varepsilon_s}{X_D} \sqrt{\frac{2N_A \varepsilon_s}{2(\Phi(0) - \Phi_D)}} \)

so \( n \) is a parameter to see how effective gate voltage is to move \( \phi(0) \).

\( n = \alpha \) (we have previously)

Once we have \( n \), we can see:

\[ \Phi(0) - \Phi_D \cdot n = V_{GS} - V_T \]

\[ \frac{\Phi(0) - \Phi_D}{kT} = \frac{\Phi(V_{GS} - V_T)}{nkT} \]

2. What is the amount of electron charge (per unit area) in the depletion region (when in subthreshold)?

Because \( n(x) = n_i e^{\frac{\Phi(x)kT}{e}} \), we could do integration

\[ Q_n(V_{GS}) = -\frac{Q}{e} \int_0^{X_D} n_i e^{\frac{\Phi(x)kT}{e}} dx \]

\[ \Phi(x) = \Phi_D + \frac{Q N_A}{2\varepsilon_s} (X_D^2 - x^2) = (\Phi(0) - \Phi_D) (1 - \frac{x}{X_D})^2 + \Phi_D \]

\[ \Phi(x) = \Phi_D + \frac{Q N_A}{2\varepsilon_s} X_D^2 (1 - \frac{x}{X_D})^2 \]

However, the integration will be complicated.

To simplify, approximate \( \Phi(x) = \Phi(0) + \frac{d\Phi(x)}{dx} \bigg|_{x=0} \cdot x \)

and do the integration.

We skip the details, one can find:

\[ Q_n(V_{GS}) = -\frac{Q}{e} \sqrt{\frac{Q N_A}{2(\Phi(0) - \Phi_D)}} \cdot \exp \left( \frac{Q (V_{GS} - V_T)}{nkT} \right) \]

(\( X \))

3. Now consider MOSFET in the subthreshold regime (weak inversion):

see Fig 3, the dotted line represent the depletion layer edge.

When applying a \( V_{GS} \), we argue that most of \( V_{GS} \) drop across the depletion region on the drain side:

\( \) (the junction on the source side is forward biased; and the body is much more

much more
As a result:
- no longitudinal electric field in channel
- electrons flow from source to drain by diffusion.

Diffusion current, \( i_D = -W \cdot D_e \frac{dQ_n}{dy} \)

If there is no recombination along channel \( \Rightarrow \) profile linearly:

\[ i_D = -W D_e \frac{Q_n(L) - Q_n(0)}{L} \]

using equation (x) from section 2

- on the source side, \( V = V_{GS} \)
  \[ Q_n(y=0) = \frac{kT}{B} \sqrt{\frac{B E_s N_A}{2(\psi(0)-\phi_p)}} \exp\left(\frac{B(V_{GS}-V_T)}{n k T}\right) \]
- on the drain side, \( V = V_{GD} \)
  \[ Q_n(y=L) = \frac{kT}{B} \sqrt{\frac{B E_s N_A}{2(\psi(0)-\phi_p)}} \exp\left(-\frac{B(V_{GD}-V_T)}{n k T}\right) \]

All together,

\[ i_D \approx -W D_e \frac{kT}{B} \sqrt{\frac{B E_s N_A}{2(\psi(0)-\phi_p)}} \left( \exp\left(\frac{B(V_{GS}-V_T)}{n k T}\right) - \exp\left(\frac{B(V_{GD}-V_T)}{n k T}\right) \right) \]

but \( i_D \) going to the left should be positive, so "-" is gone

\[ i_D \approx \frac{W}{L} \frac{\mu e (\frac{kT}{B})^2}{\phi_p} C_{DP} \exp\left(\frac{B(V_{GS}-V_T)}{n k T}\right) (1 - \exp\left(-\frac{B V_{OS}}{n k T}\right)) \]

\( V_{GD} = V_{GS} + V_{SD} = V_{GS} - V_{DS} \)

Note:
1. when \( V_{DS} = 0 \), \( i_0 = 0 \) (two sides have equal charge density)
2. when \( V_{DS} \gg \frac{kT}{B} \) (only 25mV @ R.T.)

\[ i_D \approx \frac{W}{L} \frac{\mu e (\frac{kT}{B})^2}{\phi_p} C_{DP} \exp\left(\frac{B(V_{GS}-V_T)}{n k T}\right) \]

with \( n = \phi_p \left(1 + \frac{C_{DP}}{C_{OX}}\right) \)
- If $C_{ox}$ $\uparrow$, $n \downarrow$, sharper sub-threshold (closer to 60 mV/dec, better)
- If $N_A \uparrow$, $C_{dp} \uparrow$, $n \uparrow$, softer sub-threshold (not good)
- $|V_{BS}|$, wider depletion layer, $C_{dp} \downarrow \Rightarrow n \downarrow$, sharper threshold

n reflect electrostatic competition between top gate & body (bottom gate)

$I_{off}$ for MOSFET: $I_{off} = I_D (V_{gs} = 0) \approx \frac{W}{L} \mu_e \left( \frac{kT}{e} \right)^2 C_{dp} \exp (-\frac{V_T}{nKT})$

$I_{off}$ is key goal for logic device design

To get low $I_{off}$:
1) increase $L$: but performance $\downarrow$
2) increase $V_{TH}$: but performance $\downarrow$
3) $n \downarrow$ by $N_A$: will have more "short channel effect" (DIBL)
or by increase $C_{ox}$