Yesterday we started to talk about digital circuit with MOSFET. Inverters are the most fundamental unit of digital circuits.

Today we will look at the transfer characteristic (i.e. $V_{out}$ vs $V_{in}$) of an inverter:

1. NMOS inverter with a resistor:

![Fig 1](image1)

$V_{in} = V_{DD} - i_D \cdot R$

We first realize that in this circuit, $V_{GS} = V_{in}$, $V_{PS} = V_{out}$

Also $V_{out} = V_{DD} - i_D \cdot R$

1) when $0 < V_{in} < V_T$, NMOS in cutoff, $i_D = 0$

$V_{out} = V_{DD}$

2) $V_{in} > V_T$, hence $V_{DS} > V_{GS} - V_T$ (i.e. $V_{out} > V_{in} - V_T$)

NMOS in saturation, $V_{out} = V_{DD} - i_D \cdot R = V_{DD} - \frac{KR}{2} (V_{GS} - V_T)^2 = V_{DD} - \frac{KR}{2} (V_{in} - V_T)^2$

This curve ($V_{out} = V_{DD} - \frac{KR}{2} (V_{in} - V_T)^2$, where $V_{in} > V_T$) is half of the parabola curve (see Fig 2)

3) when $V_{in} > V_T$, but $V_{DS} < V_{GS} - V_T$ (i.e. $V_{out} < V_{in} - V_T$)

NMOS in linear/triode:

$V_{out} = V_{DD} - \frac{KR}{2} (V_{in} - V_T - \frac{V_{out}}{2}) \cdot V_{out}$

we have: $\frac{KR}{2} V_{out}^2 - (KR (V_{in} - V_T) + 1) V_{out} + V_{DD} = 0$

can solve $V_{out} = \frac{KR (V_{in} - V_T) + 1 \pm \sqrt{[KR (V_{in} - V_T) + 1]^2 - 2KR V_{DD}}}{KR}$

The lowest $V_{out}$ does not reach 0, but rather $V_L = \frac{R_{on}}{R_{on} + R} \cdot V_{DD}$
where \( R_{on} = \frac{1}{K(V_{DD} - V_{T})} \)

So it is not "rail-to-rail" logic, and there are other issues (high power dissipation & low noise margin) as well.

2) Consider CMOS inverters:

\[
\begin{align*}
V_{Gsn} &= V_{IN} \\
V_{Dsn} &= V_{IN} \\
V_{SseP} &= V_{DD} - V_{IN} \\
V_{SdeP} &= V_{DD} - V_{OUT}
\end{align*}
\]

\( V_{Gsn} < V_{In} \):

- nMOS off, PMOS \( V_{SseP} \) large, PMOS on. \( \Rightarrow V_{OUT} = V_{DD} \)

5) When \( V_{DD} + V_{TP} < V_{IN} < V_{DD} \):

- PMOS \( V_{SseP} = V_{DD} - V_{IN} < V_{DD} - (V_{DD} + V_{TP}) = -V_{TP} \), PMOS cut off

but nMOS is on \( \Rightarrow V_{OUT} = 0 \)

Drawing the two boundary lines: \( V_{OUT} = V_{IN} - V_{TN} \) & \( V_{OUT} = V_{IN} + (-V_{TP}) \)

We can see that:

- region 2) & 3) are: nMOS in saturation,
- 4) & 5) nMOS in triode/linear

- region 3) & 4): PMOS in saturation
- region 2) & 1): PMOS in triode/linear

To summarize:

<table>
<thead>
<tr>
<th>PMOS</th>
<th>nMOS</th>
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<tbody>
<tr>
<td>linear</td>
<td>cut off</td>
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<td>linear</td>
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<td>cut off</td>
<td>linear</td>
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so region 3) is both pMOS & nMOS in saturation.

we have \( i_{on} = \frac{K_n}{2} (V_{in} - V_{tn})^2 \) and \( i_{op} = \frac{K_p}{2} (V_{dd} - V_{in} + V_{tp})^2 \)

let \( i_{on} = i_{op} \Rightarrow \frac{K_n}{2} (V_{in} - V_{tn})^2 = \frac{K_p}{2} (V_{dd} - V_{in} + V_{tp})^2 \)

\[ V_{in} = \frac{V_{dd} + V_{tp} + V_{tn} \sqrt{K_n/K_p}}{1 + \sqrt{K_n/K_p}} \]

If we make the device match with each other, \( K_n = K_p \) (i.e. \( \frac{W_n}{L_n} \) is larger than \( \frac{W_p}{L_p} \)), and \( V_{tn} = -V_{tp} \), we have

\[ V_{in} = \frac{V_{dd}}{2}, \quad \frac{V_{dd}}{2} - V_{tn} \leq V_{out} \leq \frac{V_{dd}}{2} - V_{tp} \]

for region 2) \& 4) we will again have parabolic segments connecting the three straight segments.

with CMOS inverter, we have rail-to-rail logic.

If time permits, will look at the small signal circuit of these inverter circuits.

1) nMOS inverter with a pull up resistor

2) CMOS inverter.