We need to size the transistors with integer \# of \( W, L \) \( (W < 20 \mu m, L < 4 \mu m) \) or Area \( (A_E < 25 A_{min} \text{ for BJT), } \mu m^2 < 25) \). \( Q_9, Q_{10}, Q_{13}, Q_{14} \) has \( L_{min} \).

1. First, let's consider voltage gain:

   **Stage 1:** From lect 21, slide #13, we find

   - Differential mode: \( |A_{v11}| = \frac{g_{m9}}{g_{o9} + 2g_{o5}} = \frac{2}{V_{A5} + V_{A9}} \frac{V_{A5} - V_{A9}}{V_{gs9} - V_{tr}} \)
   - Common mode: \( |A_{c11}| = \frac{g_{o11}}{g_{m9}} = \frac{V_{gs9} - V_{tr}}{2V_{A11}} \)

   Since \( Q_9 \) has \( L_{min} \), \( V_{A9} = 20V \), choose \( (V_{gs9} - V_{tr}) = 0.2V \). \( V_{gs9} = V_{tr} = 0.2V \) want to maximize \( |A_{v11}| \), but minimize \( |A_{c11}| \).

   | \( V_{A5} \) | \( |A_{v11}| \) | \( \Delta g \approx \Delta q \) |
   |---|---|---|
   | 20V | 100 | \( L_{min} \) |
   | 40V | 133 | \( 2L_{min} \) |
   | 60V | 150 | \( 3L_{min} \) |

   | \( V_{A11} \) | \( |A_{v11}| \) | \( \Delta g \approx \Delta q \) |
   |---|---|---|
   | 20V | 5 \times 10^{-3} | \( L_{min} \) |
   | 40V | 2.5 \times 10^{-3} | \( 2L_{min} \) |
   | 60V | 1.67 \times 10^{-3} | \( 3L_{min} \) |

2. **Stage 2:** From lect 21, slide 6

   - Differential mode: \( |A_{v21}| = \frac{2g_{m14} \times \frac{1}{2}}{g_{o16} + g_{o14}} \frac{V_{A14} - V_{A16}}{V_{A14} + V_{A16}} \)
   - Common mode: \( |A_{c21}| = \frac{g_{o12}}{g_{m14}} \frac{V_{gs16} - V_{tr}}{V_{tr}} \)

   For each case, calculate \( V_{A5}, V_{A9}, V_{A11}, V_{A14}, V_{A16}, V_{gs9}, V_{gs16} \) using the transistor sizes and bias conditions.
\[ V_{A14} = 20V \text{ (since Q4 has } L_{\text{min}} \text{), } V_{\text{os14}} - |V_T| = 0.2V \]

want to have high \(|A_{\text{ud2}}|\), but low \(|A_{\text{vd2}}|\).

\[
\begin{array}{|c|c|c|}
\hline
V_{A16} & A_{\text{ud2}} & Q_{15}, Q_{16} \\
\hline
20V & 200 & 100 \ L_{\text{min}} \\
40V & 266 & 133 \ a \ 2L_{\text{min}} \\
60V & 306 & 130 \ 3L_{\text{min}} \\
\hline
\end{array}
\]

\[
\begin{array}{|c|c|c|}
\hline
V_{A12} & A_{\text{vd2}} & Q_{17}, Q_{18}, Q_{19} \\
\hline
20V & 1 \times 10^{-2} & L_{\text{min}} \\
40V & 5 \times 10^{-3} & 2L_{\text{min}} \\
60V & 3.33 \times 10^{-3} & 3L_{\text{min}} \\
\hline
\end{array}
\]

3. Stage 3: \(|A_{v3}| \sim 1\)

4. Stage 4: \(|A_{v4}| \sim 1\)

5. Stage 5: \(|A_{v5}| = \frac{R_L}{V_{A12} g_m + R_L} = \frac{50}{50 + \frac{V_{dd}}{2 I_{23}}} < 1\) need to decide \(I_{23}\)

2. Consider \(Y_{\text{out}} \leq 10 \Omega\):

From Lecture 21, slide 25, \& slide 21, we have two paths in parallel:

(half circuit technique)

\[ Y_{os3} = \frac{1}{g_{m3}} = \frac{2 I_{B1AS3}}{V_{SA18} - |V_T|} \]

consider \(Y_{\text{out1}}\) for example:

\[
Y_{\text{out1}} = \frac{Y_{\pi23} + Y_C}{\beta_{23} + 1} \quad (\beta_{23} = \beta_n = 200)
\]

\[ \beta_C = \beta_p = 100 \]

\[ Y_{oc} \geq \frac{Y_{20} + Y_{os3}}{(\beta_{20} + 1)} \]

\[ Y_{\text{out1}} = \frac{Y_{\pi23}}{\beta_{23} + 1} + \frac{Y_{20}}{(\beta_{23} + 1)(\beta_{20} + 1)} + \frac{Y_{os3}}{(\beta_{23} + 1)(\beta_{20} + 1)} \]

\[
\alpha = \frac{1}{g_{m23}} + \frac{1}{g_m \cdot \beta_n} + \frac{1}{g_m \cdot \beta_n R_n}
\]
we should not ignore the 2nd term in \( \text{vout}_1 \), since \( I_{20} \) could be much smaller than \( I_{23} \), \( g_{m20} \ll g_{m23} \).

but estimate: \( \text{vout}_1 \approx \frac{1}{g_{m23}} \frac{V_{th}}{I_{23}} < 20 \Omega \) \( V_{th} = 25 \text{mV} \) \( \Rightarrow I_{23} \gg 1.25 \text{mA} \)

3. Power dissipation: \( \leq 9 \text{mW} \)

The current through the stages (stage 0, 1, 2, 3, 4, 5)

\[ (I_0 + I_{\text{BIAS}_1} + I_{\text{BIAS}_2} + I_{\text{BIAS}_3} + I_{\text{BIAS}_4} + I_{\text{BIAS}_5} + I_{23}) \leq 3 \text{mA} \]

(3V \leq 9 \text{mW})

And we have \( I_{23} \gg 1.25 \text{mA} \)

should try to minimize the current in the earlier stages.

From Lect 21, slide #19

\[ \frac{I_{\text{BIAS}_4}}{I_{\text{BIAS}_5}} = (\beta_p + 1)/(\beta_n + 1) \approx \beta_p/\beta_n = 1/2 \]

\( \text{Area of } Q_{21} \approx 2 \text{ Area of } Q_{20} \quad \gamma_{21} = 2 \gamma_{20} \) (try \( \gamma_{21} = 2 \gamma_{20} = \frac{1}{4} \))

\( (W/L)_{19} = (W/L)_{22} \)

From Lect 21, slide #20

\[ \frac{I_{E23}}{I_{E21}} = \frac{(\beta_i + 1) \gamma_{23} \gamma_{24}}{(\beta_p + 1) \gamma_{20} \gamma_{21}} \]

\[ \approx \frac{1}{2} \frac{\gamma_{23} \gamma_{24}}{\gamma_{20} \gamma_{21}} = \frac{1}{2} \frac{I_{E23}}{I_{E21}} \]

\[ \therefore |I_{E23}|/|I_{E24}| \text{ at } V_{out} = 0; \gamma_{24} = \gamma_{23} \]

4. \( V_{\text{REF}} \) MOSFET Diode stack.
Above: With $V_{in} = 0$, there will be a non-zero output, i.e., a DC offset, that depends on the voltage on the high impedance node.

Right: In practice, feedback is used to greatly reduce the DC offset of the output, as well as to stabilize the gain.

DC offset at the output of an Op Amp

$K(v_{out} - v_{in})^2 = K_s(v_{in} - V_{off})^2 = K_s(v_{in} - V_{off})^2$

- choose $V_{off}$ such that $K_s(v_{in} - V_{off})^2$ is negligible
- correlate with the ohm's law considerations earlier
- minimize current, minimize $V_{in}$ product