Last week we discussed on frequency response of linear amplifiers, particularly we looked at examples of CS, CE Amplifier, and we found the high frequency limit (\( \omega_{HI} \), where the gain starts to roll off) is determined by not only device parameters, but also circuit parameters (\( Ks(K_c) \), \( \gamma \), \( g_L \), \( g_m \), etc).

Devices designers often want figures of merit for their devices that are independent of any particular circuits and intrinsic to the device. Today we will look at the intrinsic high frequency limitation of the transistors. We will still use CS, CE Amps as examples.

**BJT**

1. Small Signal Circuit

   ![BJT Diagram]

   \[ C_G = g_m V_b + C_{eb} \cdot d_p = C_{eb} \cdot d_p + \left( \frac{2 I_c}{R_T} \right) \left( \frac{W_D}{2D} \right) \]

   \[ C_G = C_{eb} \cdot d_p \]

2. Intrinsic Frequency Response

   ![Intrinsic Frequency Response Diagram]

   Node 1: \( i_{in} = V_c (g_m + jw C_c) + V_c \cdot jw C \)

   Node 2: \( i_{out} = g_m V_c + jw C \cdot V_c = 0 \)

   \( i_{out} = (g_m - jw C) V_c \)

**MOSFET**

![MOSFET Diagram]

\[ V_{SB} = 0 \]

\[ g_0 V_{gs} + g_{ds} C_{gs} = 0 \]

\[ V_{gs} = \frac{2}{3} W L C_{ox} + W C_{ov} \]

\[ g_d = W C_{ov} \]

Node 1: \( i_{in} - jw C_{gs} \cdot V_{gs} - jw C_{gd} \cdot V_{gs} = 0 \)

\( \Rightarrow i_{in} = jw (C_{gs} + C_{gd}) V_{gs} \)

Node 2: \( i_{out} - jw C_{gs} + jw C_{gd} \cdot V_{gs} = 0 \)

\( \Rightarrow i_{out} = (g_m - jw C_{gd}) \cdot V_{gs} \)

\( i_{out} = \frac{g_m - jw C_{gd}}{g_m + jw (C_{gs} + C_{gd})} \cdot \frac{gm (1 - \frac{jw}{\omega_c})}{2 \pi \cdot \lambda \cdot a} \)
one pole, \( \omega_p = \frac{g_m}{C_t+C_\mu} \)

\[ \omega_p = \frac{g_m}{C_t+C_\mu} = \frac{g_m}{C_t} + \frac{g_m}{C_\mu} \]

\[ \Rightarrow \omega_p = \frac{g_m}{C_t+C_\mu} = \frac{g_m}{C_t+C_\mu} \]

3. Unit gain frequency: \( f_T \).

\[ f_T = \frac{1}{2\pi} \frac{g_m}{C_t+C_\mu} = \frac{1}{2\pi} \frac{g_m}{C_t+C_\mu} \]

\[ f_T = \frac{1}{2\pi} \frac{g_m}{C_t+C_\mu} \]

- At low collector current, \( f_T \) dominated by depletion capacitances at b-e \& b-c junctions.
- As the \( I_c \), diffusion capacitance \( g_m C_t \)
- \( g_m T_b \) becomes dominant.

\[ f_T \approx 2\pi \frac{2P}{T_b} = 2\pi \frac{2P}{T_b} = 2\pi \frac{2P}{T_b} \]

To increase \( f_T \):
- Low \( I_c \), depletion cap limited, shrink emitter \( W_e \).
- High \( I_c \), diffusion cap limited, shrink base width, use npn.

- \( f_T \) is independent of \( W \).
- If we want high \( f_T \), speed \& gain, bias well below \( V_T \) (compromise).
- Scale channel length \( L \) small as possible.
- nMOS preferred over pMOS when velocity saturation dominates.

\[ f_T = \frac{1}{2\pi} \frac{W_e g_m \mu C_{ox}}{W L C_{ox}} = \frac{S_{sat} \cdot L}{2\pi} \]

\[ \frac{1}{2\pi} \frac{1}{L \cdot \frac{1}{2\pi}} \]