• Announcements
  Stellar - Two supplemental readings posted
  Exam Two - Be the first in your living unit to study for it.

• Review – Large Signal Circuits for MOSFETs
  Strong Inversion; Sub-threshold; Velocity Saturation

• Digital building blocks - inverters
  A generic inverter
  MOS inverter options

• Digital inverter performance metrics
  Transfer characteristic: logic levels and noise margins
  Power dissipation
  Switching speed
  Fan-out, fan-in
  Manufacturability

• Comparing the MOS options
  And the winner is....
**Reviewing our LECs:** Important points made in Lec. 13

We found LECs for BJTs and MOSFETs in both strong inversion and sub-threshold. When $v_{bs} = 0$, they all look very similar:

Most linear circuits are designed to operate at frequencies where the capacitors look like open circuits. We can thus do our designs neglecting them.*

### Bias dependences:

<table>
<thead>
<tr>
<th></th>
<th>BJT</th>
<th>ST MOS</th>
<th>SI MOS</th>
<th>SI MOS w. $s_{sat}$, $\delta$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_i$</td>
<td>$qI_C/\beta FkT$</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$g_m$</td>
<td>$qI_C/kT$</td>
<td>$qI_D/nkT$</td>
<td>$\sqrt{2K_oI_D/\alpha}$</td>
<td>$W s_{sat} C_{ox}^*$</td>
</tr>
<tr>
<td>$g_o$</td>
<td>$\lambda I_C$</td>
<td>$\lambda I_D$</td>
<td>$\lambda I_D$</td>
<td>$\delta W s_{sat} C_{ox}^* = \delta g_m$</td>
</tr>
</tbody>
</table>

The LEC elements all depend on the bias levels. Establishing a known, stable bias point is a key part of linear circuit design. We use our large signal models to do this.  

*Only when we want to determine the maximum frequency to which our designs can usefully operate must we include the capacitors.*
LEC s: Identifying the incremental parameters in the characteristics

**BJT:**

\[ g_m = \frac{qI_C}{kT}; \ g_\pi = \beta g_m \quad \text{with} \quad \beta = \frac{di_C}{di_B}\big|_Q; \ g_o = \frac{di_C}{dv_{CE}}\big|_Q \]

**MOSFET:**

\[ g_m = \frac{di_D}{dv_{GS}}\big|_Q; \ g_{mb} = \eta g_m \quad \text{with} \quad \eta = \frac{-dV_T}{dv_{BS}}\big|_Q; \ g_o = \frac{di_D}{dv_{DS}}\big|_Q \]
Output conductance, $g_o$

- The finite output conductance, $g_o$, is due to Drain-Induced Barrier Lowering (DIBL), whereby the $V_T$ depends (linearly) on $V_{DS}$: $V_T = V_{To} - \delta \cdot V_{DS}$.

- Theoretically, $g_o$ should be $C_{ox}^* \cdot W \cdot s_{sat} \cdot \delta$. This is independent of $v_{GS}$ so all of the curves should parallel in saturation, and this is clearly seen in the figure.

- The slope of the orange lines is $\approx 0.3$ mA/V-µm. Using $C_{ox}^* = 2.5 \times 10^{-6}$ Coul/V-cm², $s_{sat} \approx 10^7$ cm/s, and $d = 126$ mV/V, we calculate $g_o/W = 0.315$ mA/V-µm.
Transconductance, $g_m = \frac{di_D}{dv_{GS}}$

Slope = $\frac{g_m}{W} = \frac{d(i_D/W)}{dv_{GS}} = \frac{1.5}{0.6} = 2.5$ mA/V-µm

Model: $g_m/W = C_{ox} \cdot s_{sat} = 2.5 \times 10^{-6} \times 10^7 = 2.5$ mA/V-µm
Drain induced barrier lowering, $\delta$

\[ \Delta V_T = 120 \text{ mV}, \quad \Delta V_{DS} = 95 \text{ mV} \]

DIBL, $\delta = 126 \text{ mV/V}$

Shift of $V_T$ : DIBL, $\delta = 0.12 \text{ V/0.095 V} = 126 \text{ mV/V}$
Sub-threshold slope and $n$

Subthreshold slope, $n$: $10^5$ in 500 mV = 100 mV/decade

$n = 100/60 = 1.67$
Building Blocks for Digital Circuits: *inverters*

A basic inverter

Device: on or off
Switch: open or closed

Logic gates

NOR:

<table>
<thead>
<tr>
<th>$v_A$</th>
<th>$v_B$</th>
<th>$v_{OUT}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
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<tr>
<td>0</td>
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<td>1</td>
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</tbody>
</table>

NAND:

<table>
<thead>
<tr>
<th>$v_A$</th>
<th>$v_B$</th>
<th>$v_{OUT}$</th>
</tr>
</thead>
<tbody>
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Performance metrics

- Transfer characteristic
- Logic levels
- Noise margins
- Power dissipation
- Switching speed
- Fan-in/Fan-out
- Manufacturability

Memory cell

Clif Fonstad, 10/25/12
Inverter metrics: Transfer characteristic

The transfer characteristic, \( v_{OUT} \) vs \( v_{IN} \), is found applying the large signal models at this node.

Node equation: 
\[
i_{PD} = i_{PU}
\]

\[
i_{PD} = \begin{cases} 
0^* \\
K_{PD} \left( v_{IN} - V_{T,PD} \right)^2 / 2 \\
K_{PD} \left( v_{IN} - V_{T,PD} - v_{OUT} / 2 \right) v_{OUT} \\
0 < v_{OUT} < \left[ v_{IN} - V_{T,PD} \right]
\end{cases}
\]

\( i_{PU} \): Depends on the specific pull-up device used.

For simplicity: \( \alpha = 1, \lambda = 0 \)

* Note: We can say \( i_{PD,off} \) is zero for the purpose of calculating a transfer characteristic. For power we may want to use:
\[
i_{PD,off} = I_{S,s} e^{-V_T/nV_i}
\]
**Inverter metrics:**  Transfer characteristic, cont.

**An example: NMOS**

**Pull-up: Depletion mode**  
n-channel MOSFET  
(Note: $V_{T,PU} < 0$)

**Pull-down: Enhancement mode**  
n-channel MOSFET

**Identify the regions**

\[
i_{PU} = \begin{cases} 
K_{PU} |V_{T,PU}|^2 / 2 \\
\text{when } 0 < |V_{T,PU}| < [V_{DD} - V_{OUT}] \\
K_{PU} [V_{T,PU} - (V_{DD} - V_{OUT})/2](V_{DD} - V_{OUT}) \\
\text{when } 0 < [V_{DD} - V_{OUT}] < |V_{T,PU}|
\end{cases}
\]

\[
i_{PD} = \begin{cases} 
0 \\
K_{PD} (V_{IN} - V_{T,PD})^2 / 2 \\
\text{when } 0 < [V_{IN} - V_{T,PD}] < V_{OUT} \\
K_{PD} (V_{IN} - V_{T,PD} - V_{OUT}/2)V_{OUT} \\
\text{when } 0 < V_{OUT} < [V_{IN} - V_{T,PD}]
\end{cases}
\]
Inverter metrics: Transfer characteristic, cont.

Combine the plots; write the node equation in each region and solve.

\[ 0 = K_{PU} \left[ |V_{T,PU}| - \left( V_{DD} - v_{OUT} \right)/2 \right] \left( V_{DD} - v_{OUT} \right) \]

\[ K_{PD} \left( v_{IN} - V_{T,PD} \right)^2/2 = K_{PU} \left[ |V_{T,PU}| - \left( V_{DD} - v_{OUT} \right)/2 \right] \left( V_{DD} - v_{OUT} \right) \]

\[ K_{PD} \left( v_{IN} - V_{T,PD} \right)^2/2 = K_{PU} \left| V_{T,PU} \right|^2/2 \]

\[ K_{PD} \left( v_{IN} - V_{T,PD} - v_{OUT}/2 \right) v_{OUT} = K_{PU} \left| V_{T,PU} \right|^2/2 \]

- PD off, PU lin.
- PD sat, PU lin.
- PD sat., PU sat.
- PD lin., PU sat.

Is this really vertical? Infinite A_v! Next slide.
**Inverter metrics:** Transfer characteristic, cont.

Is the characteristic really vertical and $v_{OUT}$ indeterminate when both transistors are in saturation? It is if $\lambda = 0$ (i.e. no Early effect), but we know this isn't true. We can find the slope when $\lambda \neq 0$ from an LEC analysis about the bias point

$$v_{OUT} = v_{IN} = \sqrt{K_{PU}/K_{PD}} \left( V_{T,PD} + |V_{T,PU}| \right).$$

This is the slope of the "vertical" portion.
**Inverter metrics:**

**Logic levels, noise margins**

Stage 1

Stage 2

Schematic showing pull-up and pull-down stages with voltage levels and logic transitions.

Stable solution

Unstable solution

Tipping point

NM_L

NM_H
**Inverter metrics:** Switching times (gate delay)

When the output goes from LO to HI, the load charge store must be charged through the pull-up device. When the output goes from HI to LO, it is discharged through the pull-down device.

Charging cycle:  \[ i_{\text{Charge}} = i_{PU} \]

Discharging cycle:  \[ i_{\text{Discharge}} = i_{PD} - i_{PU} \]

We can often model \( C_L \) as a linear capacitor (i.e. a multiple of \( C_{ox} \)) in which case the charge and discharge cycles are found by solving:

\[
\tau_{\text{Charge}} : \quad \frac{dv_{OUT}}{dt} = \frac{1}{C_L} i_{PU}(v_{OUT}) \\
\tau_{\text{Discharge}} : \quad \frac{dv_{OUT}}{dt} = \frac{1}{C_L} [i_{PD}(v_{IN}, v_{OUT}) - i_{PU}(v_{OUT})]
\]
Inverter metrics: Power

Total Power:

Two components - static and dynamic (switching)

\[ P_{Total} = P_{Static} + P_{Dynamic} \]

Static:

Pull-down off:

\[ P_{Static, off} = I_{PD, off} V_{DD} \quad (\approx 0) \]

Pull-down on:

\[ P_{Static, on} = I_{PU, on} V_{DD} \]

To estimate the total static power we assume the typical pull-down is off half the time and on half the time.

\[ P_{Static, ave} = \frac{1}{2} P_{Static, on} + \frac{1}{2} P_{Static, off} = \frac{1}{2} \left( I_{PD, off} + I_{PU, on} \right) V_{DD} \]
**Inverter metrics:** Power, cont.

**Dynamic:**

**Charging cycle:**

- **Pull-Up**
- $V_{DD}$
- $i_{PU}$
- $C_L$
- HI to LO
- OFF

**Discharging cycle:**

- **Pull-Up**
- $V_{DD}$
- $i_{PU}$
- $C_L$
- HI to LO
- ON

\[
\frac{1}{2} C_L V_{DD}^2 \quad \text{Dissipated,}\quad \frac{1}{2} C_L V_{DD}^2 \quad \text{Stored}
\]

Energy dissipated per cycle:

\[
\begin{aligned}
C_L V_{DD}^2 \\
\text{Cycles per second:} \quad f
\end{aligned}
\]

\[
P_{\text{Dynamic, ave}} = f C_L V_{DD}^2
\]

**Total:**

\[
P_{\text{Total}} = \frac{1}{2} \left( I_{PD,off} + I_{PU,on} \right) V_{DD} + f C_L V_{DD}^2
\]
MOS inverters:
5 pull-up choices

Generic inverter

Resistor pull-up

n-channel, e-mode pull-up*

Active p-channel pull-up (CMOS)**

n-channel, d-mode pull-up (NMOS)

* Called PMOS when made with p-channel FETs.
** Notice that CMOS has a larger (~3x) input capacitance.
MOS inverters: Comparing the 5 pull-up choices

Ground rules:

To make the comparison meaningful, we set the following conditions:

1. We use the same pull-down device with each of the different pull-ups.

2. We use the same fan out, $n$, to identical inverters to have a valid comparison of the amount of charge that must managed to charge and discharge, and of the dynamic power dissipation. We also assume the load capacitance, $C_L$, is linear and $n$ times a single inverter input capacitance.

3. We use the same $V_{HI}$ and $I_{PU, on}$ so the static power dissipation is the same.

In this way we can see which pull-up gives us the highest speed, all else being equal.
Switching transients

General approach

The load, $C_L$, is a non-linear charge store, but for MOSFETs it is fairly linear and it is useful to think linear:

$$\frac{dv_{OUT}}{dt} = i_L(v_{OUT})/C_L$$

Charging $C_L$:
The charging current for the various MOSFET pull-up options

$\text{CMOS, } I_{ON} = 0$

$\text{n-ch, d-mode}$

Resistor and $\text{n-ch, e-mode w. } V_{GG} \text{ on gate}$

$\text{n-ch, e-mode } V_{DD} \text{ on gate}$

Bigger current $\rightarrow$ faster $v_{OUT}$ change
Switching transients, cont.

Discharging $C_L$:
This depends on the pull-up device, as well as the pull-down.
The discharging current for the various pull-up options

\[ i_{PD} = i_{\text{Discharge}} + i_{PU} \]

Discharging cycle:
\[ i_{\text{Discharge}} = i_{PD} - i_{PU} \]

\[ \begin{align*}
  &\text{n-ch, d-mode} \\
  &\text{n-ch, e-mode w. } V_{GG} \text{ on gate} \\
  &\text{resistor and n-ch, e-mode} \\
  &\text{CMOS (} i_{PU} = 0 \text{)} \\
\end{align*} \]

\checkmark The discharge current ($i_{\text{Discharge}}$) is the difference between the upper curve ($i_{PD}$) and the appropriate lower curve ($i_{PU}$).

Which pull-up is best? To see we next look at each in turn and then compare them.
Switching transients, cont.

Charging and discharging: Linear resistor pull-up

Simple
Least costly with discrete components but integrated resistors consume lots of space.

\[ i_{PU} = i_{\text{Charge}} \]

\[ i_{PD} = i_{\text{Discharge}} + i_{PU} \]

\[ \tau_{\text{Charge}} \gg \tau_{\text{Discharge}} \]
Switching transients, cont.

Charging and discharging: Saturated E-mode pull-up

No added cost in adding more MOSFETs
Very compact
No added wiring
Slower than linear resistors

\[ i_{PU} = i_{Charge} \]
\[ i_{PD} = i_{Discharge} + i_{PU} \]

\[ \tau_{Charge} \gg \gg \gg \tau_{Discharge} \]
Switching transients, cont.

Charging and discharging:
Linear E-mode pull-up

\[ \text{Charging:} \quad i_{\text{PD}} = i_{\text{Discharge}} + i_{\text{PU}} \]

\[ \tau_{\text{Charge}} \gg \tau_{\text{Discharge}} \]

Still compact
Need to wire VGG to each gate
Need second supply
Not faster than linear resistor

\[ V_{\text{DD}} \]

\[ V_{\text{GG}} (\gg V_{\text{DD}}) \]

\[ V_{\text{IN}} \]

\[ V_{\text{OUT}} \]

\[ i_{\text{PU}} = i_{\text{Charge}} \]

\[ i_{\text{ON}} \]

\[ i_{\text{PD}} = i_{\text{Discharge}} + i_{\text{PU}} \]

\[ i_{\text{Charge}} \]

\[ V_{\text{OUT}} \]

\[ V_{\text{DD}} \]
Switching transients, cont.

Charging and discharging:
D-mode pull-up ("NMOS")

\[ V_{OUT} = V_{DD} + i_{Discharge} + i_{PU} \]

\[ V_{IN} = V_{DD} + i_{Charge} \]

Compact
Symmetrical charge/discharge
Fastest possible
Must make E- and D-mode on safe wafer

\[ \tau_{Charge} \approx \tau_{Discharge} \]
Switching transients, cont.

Charging and discharging:
Active complementary pull-up
("CMOS")

Symmetrical charge/discharge
Almost as fast, or even faster than, n-MOS*
Minimal static power dissipation ($I_{ON} \approx 0$)
Must make n- and p-channel on same wafer

\[ I_{PU} = I_{Ch} \]

\[ I_{PD} = I_{Dh} + I_{PU} \]

\[ \tau_{Charge} \approx \tau_{Discharge} \]

* The input capacitance is 3x larger, but the interconnect capacitance is the same, so it depends on which of the two is dominant.
Switching transients: summary of charge/discharge currents

Resistor and E-mode pull-up ($V_{GG}$ on gate)

E-mode pull-up ($V_{DD}$ on gate)

D-mode pull-up (called "NMOS")

CMOS

- Comparisons made with same pull-down MOSFET, $V_{HI}$, and $I_{ON}$.
MOS Technology: An abbreviated history

p-MOS:
In the beginning (mid-60s) there were only metal-gate p-channel e-mode MOSFETs; n-channel MOSFETs came out d-mode. p-MOS logic relied on saturated and linear e-mode pull-ups.

n-MOS:
With the development of <100> substrates, e-beam deposition, self-aligned poly-Si gates, and ion implantation, initially to improve p-MOS, it became possible to also reliably fabricate e-mode n-channel FETs. NMOS, with d-mode pull-ups, then took off (ca 1970).

CMOS:
It was clear for many years that CMOS inverters were superior, but fabricating them reliably in high density and at low cost was a big challenge. Eventually manufacturers learned how to make n- and p-channel MOSFETS together in close proximity and economically (ca 1980); CMOS then soon became the dominant IC technology because of its superior low power and high speed.

For the past decade the industry has been fixated on systematically making FETs smaller, circuits more dense, and wafers larger.*

* And with good reason; more later in Lectures 16 and 26.
Lecture 14 - Digital Circuits: Inverter Basics - Summary

• Digital building blocks - inverters
  A generic inverter: Switch = pull-down device, Load = pull-up device
  MOS inverter options - Pull-down: n-channel, e-mode (faster than p-channel)
  Pull-up: 1. resistor; 2. n-channel, e-mode w. and w.o. gate bias;
           3. n-channel, d-mode (NMOS); 4. p-channel, e-mode (CMOS)

• Digital inverter performance metrics
  Transfer characteristic
    Logic levels: $V_{HI}$, $V_{LO}$
    Noise margins: $NM_{HI}$ (high), and $NM_{LO}$ (low)
    Design variables: choice of pull-up device
                      pull-up and pull-down thresholds
                      device sizes (absolute and relative)
  Power dissipation: stand-by power and switching dissipation
  Switching speed: capacitive load
                   charge and discharge currents critical
  Fan-out, fan-in: minimal issue in MOS; more so with BJT logic
  Manufacturability: small, fast, low-power, reliable, and cheap

• Comparing the MOS options
  And the winner is….CMOS