Lecture 24 - Intrinsic Limits of Transistor Speed - Outline

• Announcements
  Final Exam – Monday, Dec 17, 9:00 am - 12 noon, Walker Mem (W30)

• Review - Shunt feedback capacitances: $C_\mu$ and $C_{gd}$
  The Miller effect: any C bridging a gain stage looks bigger at the input
  Marvelous cascode: CE/S-CB/G (E/SF-CB/G work, too - see µA741)
    large bandwidth, large output resistance
    used in gain stages and in current sources
  Using the Miller effect to advantage: Stabilizing OP Amps - the µA741

• Intrinsic high frequency limitations of transistors
  General approach
  MOSFETs: $f_T$
    biasing for speed
    impact of velocity saturation
    design lessons
  BJT: $f_\beta$, $f_T$, $f_\alpha$
    biasing for speed
    design lessons
Summary of **OCTC** and **SCTC** results

- **OCTC**: an estimate for $\omega_{HI}$
  1. $\omega_{HI}^*$ is a weighted sum of $\omega$'s associated with **device capacitances**:
     (add RC's and invert)
  2. Smallest $\omega$ (largest RC) dominates $\omega_{HI}^*$
  3. Provides a lower bound on $\omega_{HI}$

- **SCTC**: an estimate for $\omega_{LO}$
  1. $\omega_{LO}^*$ is a weighted sum of $\omega$'s associated with **bias capacitors**:
     (add $\omega$'s directly)
  2. Largest $\omega$ (smallest RC) dominates $\omega_{LO}^*$
  3. Provides an upper bound on $\omega_{LO}$
The Miller effect (general)

Consider an amplifier shunted by a capacitor, and consider how the capacitor looks at the input and output terminals:

\[ i_{in} = C_m \frac{d[(1 - A_v)v_{in}]}{dt} = (1 - A_v)C_m \frac{dv_{in}}{dt} \]

Note: \( A_v \) is negative

\[ C_m \frac{(1 - A_v)}{A_v} \approx C_m \]

\( v_{out} = A_v v_{in} \)

\( C_{in} \) looks much bigger than \( C_m \)

\( C_{out} \) looks like \( C_m \)
The cascode when the substrate is grounded:

High frequency issues:

**L.E.C. of cascode:** can't use equivalent transistor idea here because it didn't address the issue of the C's!

Voltage gain $\approx -1$ so minimal Miller effect.

Voltage gain $\approx g_m r_l$, without Miller effect.

Common-source gain without the Miller effect penalty!
Multi-stage amplifier analysis and design: The µA741

Figuring the circuit out:

- Current mirror load
- Emitter-follower/common-base "cascode" differential gain stage
- Darlington common-emitter gain stage
- Push-pull output
- Simplified schematic

The full schematic
Multi-stage amplifier analysis and design: Understanding the µA741 input "cascode"

Begin with the BJT building-block stages:

- **Common base**
  - $i_{in} \approx (g_m + g_\pi)$
  - $i_{out} \approx g_o / \beta$

- **Common emitter**
  - $i_{in}$
  - $V_{in}$
  - $V_{out}$
  - $g_m v_\pi$
  - $g_o$
  - $g_{m, \pi}$

- **Emitter follower**
  - $i_{in}$
  - $V_{in}$
  - $V_{out}$
  - $g_{sl}$
  - $\beta / (r_t + r_\pi)$

Relative sizes:
- $g_m$: large
- $g_\pi$: medium
- $g_o$: small
- $g_t, g_i$: cannot generalize

Clif Fonstad, 12/4/12
Multi-stage amplifier analysis and design: Two-port models

Two different bipolar "cascode" configurations:

In a bipolar cascode, starting with an emitter follower reduces the overall gain by $\approx 2x$, but it also gives twice the input resistance, which is helpful.
Multi-stage amplifier analysis and design: MOSFET 2-port models

Reviewing our building-block stages:

- **Source follower**
  - $i_{in} = g_m v_{in}$
  - $v_{out} = g_m v_{in} + g_o (g_m + g_{mb}) v_{in}$
  - $r_t$, $i_{out}$

- **Common gate**
  - $i_{in} = g_m v_{in}$
  - $v_{out} = g_m v_{in} + g_o g_t v_{in}$
  - $r_t$, $i_{out}$

- **Common source**
  - $v_{out} = g_m v_{in}$
  - $i_{in} = g_m v_{in}$
  - $r_l = 1/g_l$

Relative sizes:
- $g_m$, $g_{mb}$: large
- $g_o$: small
- $g_t$, $g_l$: cannot generalize
Multi-stage amplifier analysis and design: Two-port models

Two different MOSFET "cascode" configurations:

With MOSFETs, starting a cascode with a source follower costs a factor of two in gain because \( r_{\text{out}} \) for an SF is small, and \( r_{\text{in}} = \infty \) anyway, so it isn't very attractive.
Multi-stage amplifier analysis and design: The µA741

The circuit: a full schematic

The monolithic capacitor made the µA741 "complete" and a big success. Why is it needed? What does it do?

C₁ is in a Miller position across Q₁₆.
Multi-stage amplifier analysis and design: The µA741

Why is there a capacitor in the circuit?: the added capacitor introduces a low frequency pole that stabilizes the circuit.

Without it the gain is still greater than 1 when the phase shift exceeds 180° (dashed curve). This can result in positive feedback and instability.

With it the gain is less than 1 by the time the phase shift exceeds 180° (solid curve).
**Intrinsic performance - the best we can do**

We've focused on $\omega_{HI}$, the upper limit of mid-band, but even when $\omega > \omega_{HI}$ the $|A_v| > 1$, and the circuit is useful. For example, for the common source stage we had

$$A_v(j\omega) = \frac{-g_t(g_m - j\omega C_{gd})}{\left[(j\omega)^2 C_{gs} C_{gd} + j\omega\left[(g_l + g_o) C_{gs} + (g_l + g_o + g_t + g_m) C_{gd}\right] + (g_l + g_o) g_t\right]}$$

A Bode plot of $A_v$ is shown to the right:

When we look for a metric to compare the ultimate performance limits of transistors, we make note of this and ask how high can a device in isolation have provide voltage or current gain?
**Intrinsic performance - the best we can do, cont.**

Consider the two possibilities shown below, one for a voltage input and output where the metric would be the open circuit voltage gain, $A_{v,oc}$, and the other for a current input and output with the metric being the short circuit current gain, $A_{i,sc}$ (commonly written $\beta_{sc}$):

![Circuit Diagram](image)

$$A_{v,oc}(s) \equiv \frac{v_{out}(j\omega)}{v_{in}(j\omega)} = -\frac{g_m - j\omega C_{gd}}{g_o - j\omega C_{gd}}$$

$$\beta_{sc}(j\omega) = \frac{i_d(j\omega)}{i_g(j\omega)} = \frac{g_m - j\omega C_{gd}}{j\omega(C_{gs} + C_{gd})}$$

Of these two alternatives, $\beta_{sc}$ is the more useful. $A_{v,oc}$ is derived with a voltage source driving a capacitor, something that doesn't give a meaningful result and leads to ever increasing input power. It also does not involve $g_m$ and $C_{gs}$. Consequently, short circuit current gain is used as the intrinsic high frequency performance metric for transistors.
The common-source short-circuit current gain is:

\[ \beta_{sc}(j\omega) \equiv \frac{i_d(j\omega)}{i_g(j\omega)} = \frac{g_m - j\omega C_{gd}}{j\omega(C_{gs} + C_{gd})} \]

there is one pole at \( \omega = 0 \), and one zero, \( \omega_z \):

\[ \omega_z = \frac{g_m}{C_{gd}} \]

The short circuit current gain, \( \beta_{sc} \), is infinite at DC (\( \omega = 0 \)), and its magnitude decreases linearly with increasing frequency.
The magnitude of $\beta_{sc}$ decreases with $\omega$, but it is still greater than one for a wide range of frequencies.

$$|\beta_{sc}(j\omega)| = \sqrt{\frac{g_m^2 + \omega^2 C_{gd}^2}{\omega^2 (C_{gs} + C_{gd})^2}}$$

The transistor is useful until $|\beta_{sc}|$ is less than one. The frequency at which this occurs is called $\omega_t$. Setting $= 1$ and solving for $\omega_t$ yields:

$$\omega_t = \sqrt{\frac{g_m^2}{(C_{gs} + C_{gd})^2 - C_{gd}^2}} \approx \frac{g_m}{C_{gs} + C_{gd}}$$
MOSFET short-circuit current gain, $\beta_{sc}(j\omega)$, cont.

- **Unity gain point**, $\omega_t$:
  $$\omega_t \approx \frac{g_m}{C_{gs} + C_{gd}}$$

- **No 3dB point**, $\omega_b$.

- **Low frequency value**: infinity

- **Zero**, $\omega_z$:
  $$\omega_z = \frac{g_m}{C_{gd}}$$

- **Note**: $\omega_z > \omega_t$
MOSFET short-circuit current gain, $\beta_{sc}(j\omega)$, cont.

Can we bias to maximize $\omega_t$?

$$\omega_t(MOSFET) = \frac{g_m}{(C_{gs} + C_{gd})} \approx \frac{g_m}{C_{gs}}$$

$$= \frac{W}{L} \mu_{Ch} C_{ox}^* |V_{GS} - V_T|$$

$$\approx \frac{2}{3} W LC_{ox}^*$$

$$= \frac{3}{2} \mu_{Ch} |V_{GS} - V_T|$$

Maximize $V_{GS}$.

What is the ultimate limit?

$$\omega_t(MOSFET) = \frac{3}{2} \mu_{Ch} \frac{|V_{GS} - V_T|}{L^2}$$

$$= \frac{3}{2L} \mu_{Ch} \frac{|V_{DS}|}{L}$$

$$= \frac{3}{2L} \mu_{Ch} \frac{E_{Ch}}{L}$$

$$= \frac{3}{2} \frac{s_{Ch}}{L}$$

$$= \frac{1}{\tau_{Ch}}$$

Lessons: Bias at well above $V_T$; make $L$ small, use n-channel.

Clif Fonstad, 12/4/12
An aside: looking back at CMOS gate delays

CMOS: switching speed; minimum cycle time (from Lec. 15)

Gate delay/minimum cycle time:

For MOSFETs operating in strong inversion, no velocity saturation:

\[ \tau_{Min\ Cycle} = \frac{12nL_{min}^2 V_{DD}}{\mu_e [V_{DD} - V_{Tn}]^2} \]

Comparing this to the channel transit time:

\[ \tau_{Ch\ Transit} = \frac{L_{min}}{\bar{s}_{e,Ch}} = \frac{L_{min}}{\mu_e E_{Ch}} = \frac{L_{min}}{\mu_e (V_{DD} - V_{Tn})/L_{min}} \]

We see that the cycle time is a multiple of the transit time:

\[ \tau_{Min\ Cycle} = \frac{12nV_{DD}}{(V_{DD} - V_{Tn})} \tau_{Channel\ Transit} = n' \tau_{Channel\ Transit} \]

When velocity saturation dominated, we found the same thing:

\[ \tau_{Min\ Cycle} \propto \frac{L_{min} V_{DD}}{S_{sat} [V_{DD} - V_{Tn}]} = n' \tau_{Chan\ Transit} \quad \text{where} \quad \tau_{Chan\ Transit} = \frac{L}{S_{sat}} \]
Intrinsic $\omega_{HI}$'s for MOSFETs - $\beta_{sc}(j\omega)$ and $\omega_t$ w. velocity saturation

What about the intrinsic $\omega_{HI}$ of a MOSFET operating with full velocity saturation?

The basic result is unchanged; we still have:

$$\omega_t = \sqrt{\frac{g_m^2}{(C_{gs} + C_{gd})^2 - C_{gd}^2}} \approx \frac{g_m}{C_{gs}(C_{gs} + C_{gd})} \approx \frac{g_m}{C_{gs}}$$

However, now $g_m$ is different:

$$g_m = W s_{sat} C_{ox}^*$$

With this we have:

$$\omega_t \approx \frac{g_m}{C_{gs}} = \frac{W s_{sat} C_{ox}^*}{W L C_{ox}^*} = \frac{s_{sat}}{L} = \frac{1}{\tau_{Ch}}$$

In the case where velocity saturation dominates, we once again find that it is the channel transit time that is the ultimate limit.

Do you care to speculate on the intrinsic $\omega_{HI}$ of a BJT?
Intrinsic $\omega_{Hi}$'s for BJTs - short-circuit current gain

The common-emitter short-circuit current gain is:

$$
\beta_{sc}(j\omega) \equiv \frac{i_c(j\omega)}{i_b(j\omega)} = \frac{g_m - j\omega C_\mu}{g_\pi + j\omega(C_\pi + C_\mu)}
$$

there is one pole, call it $\omega_p$, and one zero, $\omega_z$:

$$
\omega_p = \frac{g_\pi}{C_\pi + C_\mu}, \quad \omega_z = \frac{g_m}{C_\mu}
$$

Of these two, $\omega_p$ is much smaller and this is the 3dB point of the common-emitter short-circuit current gain. We give it the name $\omega_\beta$:

$$
\omega_\beta = \frac{g_\pi}{C_\pi + C_\mu}
$$
The magnitude of $\beta_{sc}$ decreases above $\omega_b$, but it is still greater than one initially:

$$|\beta_{sc}(j\omega)| = \sqrt{\frac{g_m^2 + \omega^2 C^2}{g^2 + \omega^2 (C_\pi + C_\mu)^2}}$$

The transistor is useful until $|\beta_{sc}|$ is less than one. The frequency at which this occurs is called $\omega_t$. Setting $= 1$ and solving for $\omega_t$ yields:

$$\omega_t = \sqrt{\frac{(g_\pi^2 + g_m^2)}{(C_\pi + C_\mu)^2 - C_\mu^2}} \approx \frac{g_m}{C_\pi + C_\mu}$$
BJT short-circuit current gain, $\beta_{sc}(j\omega)$, cont.

Unity gain point, $\omega_t$: $\omega_t \approx g_m/(C_{\pi} + C_{\mu})$

3dB point, $\omega_b$: $\omega_b = g_m/(C_{\pi} + C_{\mu})$

Low frequency value: $\beta_F$

Zero, $\omega_z$: $\omega_z = g_m/C_{\mu}$

Note: $\omega_z > \omega_t >> \omega_\beta = \omega_t/\beta_F$
BJT short-circuit current gain, $\beta_{sc}(j\omega)$, cont.

Can we bias to maximize $\omega_t$?

$$\omega_t \approx \frac{g_m}{(C_\pi + C_\mu)} = \frac{qI_C}{kT} \left( \frac{qI_C}{kT} \tau_b + C_{eb,dp} + C_{cb,dp} \right)$$

Maximize $I_C$.

Used $C_\pi = g_m \tau_b + C_{eb,dp}$

Lessons: Bias at large $I_C$; make $w_B$ small, use npn.

In the limit of large $I_C$:

$$\lim_{I_C \to \infty} \omega_t \approx \frac{1}{\tau_b} = \frac{2D_{\text{min,B}}}{W_B^2} = \frac{2\mu_{\text{min,B}} V_{\text{thermal}}}{W_B^2}$$
Lecture 24 - Intrinsic Limits of Transistor Speed - Summary

• Intrinsic high frequency limits for transistors
  **General approach:** short-circuit current gains

• Limits for MOSFETs:
  **Metric - CS short-circuit current unity gain pt:** \( \omega_T = \frac{g_m}{(C_{gs} + C_{gd})^2 - C_{gd}^2} \)
  \( \omega_T \) is approximately \( \frac{g_m}{C_{gs}} = \frac{3\mu_e(V_{GS} - V_T)}{2L^2} \)
  \( g_m = (W/L)\mu_e C_{ox}^* (V_{GS} - V_T) \) and \( C_{gs} = \frac{2}{3}WLC_{ox}^* \)
  so \( \omega_T \approx \frac{3\mu_e(V_{GS} - V_T)}{2L^2} = \frac{1}{\tau_{ch}} \)
  **Design lessons:** bias at large \( I_D \)
  minimize \( L \) (win as \( L^2 \); as \( L \) in velocity saturation)
  use n-channel rather than p-channel \( (\mu_e >> \mu_h) \)

• Limits for BJTs:
  **Metrics - CE short-circuit current gain 3dB pt:** \( \omega_b = \frac{g_p}{(C_{\pi} + C_{\mu})} \)
  **CE short-circuit current gain unit gain pt:** \( \omega_T = \frac{g_m}{(C_{\pi} + C_{\mu})} \)
  \( \omega_T \) approaches \( 1/\tau_b \) as \( I_c \) increases and \( \tau_b = w_B^2/2D_{min,B} \)
  so \( \omega_T \approx 2D_{min,B}/w_B^2 = 2\mu_e V_t/w_B^2 = \frac{1}{\tau_b} \)
  **CB short-circuit current gain unit gain pt:** \( \omega_\alpha = \frac{g_m}{C_{\pi}} \)
  **Design lessons:** bias at high collector current
  minimize \( w_B \) (win as \( w_B^2) \)
  use npn rather than pnp \( (\mu_e >> \mu_h) \)