Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology

6.012 Electronic Devices and Circuits

FINAL EXAMINATION

Monday, December 15, 2003
duPont Center Gymnasium, 9:00 am to Noon
Closed Book - Formula sheet provided; 3-page crib sheet permitted

Notes:

1. Unless otherwise indicated, assume room temperature and use: \( q = 1.6 \times 10^{-19} \) Coul, \( kT/q = 0.025 \) V, \( (kT/q) \ln 10 = 60 \) mV, and \( n_i = 10^{10} \) cm\(^{-3}\) for Si.

2. This test is designed so that most parts can be worked independently of the others.

3. All of your answers and any relevant work must appear on these pages. Any additional paper you hand in will not be graded.

4. Make reasonable approximations and assumptions. State and justify any such assumptions and approximations.

5. Be certain that you have all fourteen (14) pages of this exam booklet and make certain that you write your name at the top of this page as indicated.


Grader Use Only

PROBLEM 1 ________ (out of 40 possible)
PROBLEM 2 ________ (out of 40 possible)
PROBLEM 3 ________ (out of 40 possible)
PROBLEM 4 ________ (out of 40 possible)
PROBLEM 5 ________ (out of 40 possible)
TOTAL ________ (out of 200 possible)
Problem 1 (40 points)

This problem concerns the silicon abrupt p-n junction diode pictured below. In this diode at room temperature the electron mobility, \( \mu_e \), is 1500 cm\(^2\)/V-s; the hole mobility, \( \mu_h \), is 600 cm\(^2\)/V-s; there is negligible recombination; and the intrinsic carrier concentration, \( n_i \), is 10\(^{10} \) cm\(^{-3}\). Throughout this problem you may assume low level injection and you may neglect the depletion region widths, i.e., \( x_n \ll w_n \) and \( x_p \ll w_p \). The cross-sectional area is 10\(^{-4} \) cm\(^2\). Notice that the figure indicates that \( w_n \) is 10 \( \mu \)m.

![Diagram of the diode with labels and equations]

3. (a) [4 points] If this diode was designed to have \( J_p(0) = 5 J_n(0) \) when bias is applied to it, how wide is the p-side, \( w_p \)?

\[
J_p = J_n \quad \Rightarrow \quad \frac{\partial n(0)}{\partial x} = \frac{n_i(0)}{W} \quad \Rightarrow \quad W_p = W_n
\]

(b) [8 points] On the axes provided below, sketch and label \( J_n(x) \), \( J_p(x) \), and \( J_{tot}(x) \), for \( -w_p < x < 10 \mu \)m when \( J_n(-x_p) \) is 1 A/cm\(^2\). Recall from Part (a) that \( J_p(0) \) is 5 \( J_n(0) \).

![Graph of currents vs. x]

Problem 1 continues on the next page
Problem 1 continued

c) [4 points] Find the value of the applied bias, $V_{AB}$, that results in a hole concentration just to the right of the edge of the space charge layer on the n-side (i.e. just to the right of $x_n$) of $10^{15}$ cm$^{-3}$.

\[ V_{ab} = \frac{KT}{q} \ln \left( \frac{n_i}{n_0} \right) \]

\[ = \frac{25 mV \ln 10^{15}}{10^{-9}} = 6.56 V \]

\[ V_{AB} = 6.56 V \]

d) [4 points] With the bias condition of Part (c), what are the total hole and electron populations on the n-side of this diode?

\[ \Phi_{tot} = \frac{1}{2} \int n(x) dx \]

\[ \Phi_{tot} = \frac{1}{2} \int (10^{15}) dx = 5 \times 10^9 \]

\[ n_{tot} = \Phi_{tot} \times 10^{15} \times 10^{-3} \times 10^4 = 5 \times 10^9 + 10^9 = 1.05 \times 10^{10} \]

\[ \pi_{TOT} = 1.05 \times 10^9 \] electrons

\[ \pi_{TOT} = 5 \times 10^9 \] holes

e) [4 points] What is the diode current density, $j_D/A$, under the bias condition of Part c)?

\[ j_D = q \left( \frac{D_n n(x)}{n_p} + D_h \frac{\Phi(x)}{n_p} \right) \]

\[ = 0.028 \times 10^{-4} \times 4 \times 10^{15} = 2.8 \times 10^{-4} \]

\[ j_D/A = 2.8 \times 10^{-4} \] Amps/cm$^2$

f) [16 points] Compare two diodes, like that pictured on page 2, which are identical except that the cross-sectional area of one, Diode A, is twice that of the other, Diode B. Both are biased to have the same terminal current, $I_D$.

i) Across which diode, if any, is the bias voltage, $V_{AB}$, larger and why?

☐ Diode A (the bigger one) ☒ Diode B ☑ They are comparable

because: Smaller area needs larger voltage for same current.

Problem 1 continues on the next page
Problem 1 continued

ii) Which diode, if any, has the larger incremental resistance, \( r_d \), and why?

( ) Diode A (the bigger one)  ( ) Diode B  (✓) They are comparable

because:

\[ r_d = \frac{kT}{q I_d} \]

iii) Which diode, if any, has the larger incremental depletion capacitance, \( C_{dp} \), and why?

(✗) Diode A (the bigger one)  ( ) Diode B  ( ) They are comparable

because:

\[ C_{dp} \]

iv) Which diode, if any, has the larger incremental diffusion capacitance, \( C_{df} \), and why?

( ) Diode A (the bigger one)  ( ) Diode B  (✗) They are comparable

because:

\[ C_{df} \propto I_d \]

End of Problem 1
Problem 2 - (40 points)

You are a device engineer in a semiconductor company (Letni Inc.). Your process engineer informs you that he mistakenly used n-type silicon substrates rather than p-type when he fabricated your n-MOSFETS, and consequently, the structure below resulted. The electrostatic potential of the heavily doped n-Poly, which is used as the gate metal, is the same as that of similarly doped crystalline silicon. Model the n-Poly as a metal with this electrostatic potential.

Your boss asks you to do some measurements on the devices to see if the process engineer is right, and that having the wrong type substrate is the only problem with them. You decide that the first thing to do is to calculate what you should see if you do C-V measurements and I-V measurements on the devices, assuming they were indeed fabricated on n-type substrates.

a) Your first step is to consider doing a CV measurement. For this measurement you will tie the source, drain and body terminals together and ground them. You will then measure the small-signal capacitance versus bias voltage curve between the gate and the body terminals.

i) [8 points] What are the flatband voltage, $V_{FB}$, and threshold voltage, $V_t$, you would expect from the structure above?

\[
V_{FB} = -\Phi_B = -(\Phi_m - \Phi_n) = - (0.54 - 0.42) = -0.12
\]

\[
V_t = V_{FB} - 2\Phi_n - \frac{1}{C_{ox}} \sqrt{2q \varepsilon Si N_D (2\Phi_n)}
\]

\[
\Phi_n = 0.42 \text{ V}
\]

\[
C_{ox} = 2.30 \times 10^{-7} \text{ F/cm}^2
\]

\[
V_{FB} = -0.12 \text{ Volts}
\]

\[
V_t = -1.68 \text{ V} \text{ Volts}
\]
ii) [4 points] On the axes provided below sketch the C-V characteristics you would expect to measure on the device indicating the values of $V_{FB}$ and $V_{T,DR}$, and the maximum value of capacitance.

![C-V Characteristics Diagram]

$$C_{OX} = 2.3 \times 10^{-7} \text{ F/cm}^2$$

iii) [6 points] For what range of gate voltages is the device in inversion, and what is the expression for the channel charge per unit area $Q_{INV}$?

$$Q_{INV} = - C_{OX} (V_{GS}-V_{T}) = -2.3 \times 10^{-7} \text{(m}^2\text{)}$$

iv) [6 points] For what range of gate voltages is the device in accumulation, and what is the expression for the channel charge per unit area $Q_{ACCUM}$?

$$Q_{ACCUM} = - C_{OX} (V_{GS}-V_{FB}) = -2.3 \times 10^{-7} \text{(m}^2\text{)}$$

b) You next consider measuring the I-V characteristics of the device as a MOSFET. The body will be tied to the source and the source will be grounded i.e. $V_{BS}=0 \text{ V}$. Assume that the channel length is $L$, with $L >> 0.1 \mu\text{m}$, and the gate width is $W$.

i) [4 points] Derive an algebraic expression for the drain current, $i_D$, of the device shown on Page 5 as a function of the gate-to-source voltage, $V_{GS}$ when the gate-source voltage is such that the channel is accumulated. Assume that drain-to-source voltage, $V_{DS}$, is small and positive (e.g., $V_{DS} = +0.05 \text{ V}$). [Hint: Notice that there are two conducting paths in parallel.]

$$i_D = i_D^{acc} + i_D^{bulk} = i_D$$

$$= p_c l_c \frac{W}{L} \left[ (V_{GS}-V_{FB}) - \frac{1}{2} V_{DS} \right] V_{DS} + q \frac{p_c}{L} W^* t \times V_{DS}$$

$t = 1000 \text{ nm}$

$$\text{Amps}$$

Problem 2 continues on the next page
ii) [4 points] Derive an algebraic expression for the drain current, \( i_D \), of the device shown on Page 5 as a function of the gate-to-source voltage, \( V_{GS} \), when the gate-source voltage is such that the channel is depleted (but not inverted). Assume that drain-to-source voltage, \( V_{DS} \), is small and positive (e.g., \( V_{DS} = 0.05 \) V). [Hint: The depletion region does not conduct; it is insulating.]

\[
i_D = \frac{q}{L} \mu_e N_D \frac{W}{L} \left[ t - X_d(V_{GS}) \right] V_{DS}
\]

\[
X_d(V_{GS}) = \frac{\varepsilon_s}{\varepsilon_0} \left[ \frac{1 + \frac{2 \sigma \varepsilon_s^2 (\phi_B + V_{gs})}{\varepsilon_s \varepsilon_0 N_A}}{1} - 1 \right]
\]

\[
i_D = \frac{q}{L} \mu_e N_D \frac{W}{L} \left[ \frac{t}{V_{DS}} \right] \text{ Amps}
\]

iii) [4 points] Derive an algebraic expression for the drain current, \( i_D \), of the device shown on Page 5 as a function of the gate-to-source voltage, \( V_{GS} \), when the gate-source voltage is such that the channel is inverted. Assume that drain-to-source voltage, \( V_{DS} \), is small and positive (e.g., \( V_{DS} = 0.05 \) V).

\[
i_D = \frac{q}{L} \mu_e N_D \frac{W}{L} \left[ \frac{t - X_{d_{max}}}{V_{DS}} \right]
\]

\[
= \frac{q}{L} \mu_e N_D \frac{W}{L} \left[ \frac{1000 \text{nm} - 104 \text{nm}}{V_{DS}} \right] \times 10^{-7}
\]

\[
i_D = \frac{q}{L} \mu_e N_D \frac{W}{L} \left[ \frac{t}{V_{DS}} \right] \text{ Amps}
\]

iv) [4 points] How would the magnitude of the Early voltage of the device shown above compare to a regular n-MOSFET? Explain your answer.

- Larger than
- Smaller than
- Similar to a regular n-MOSFET

because

parallel conduction path underneath leads to very small large output conductance

\[
\frac{d}{V_A}
\]

End of Problem 2

\[
i_D = \frac{q}{L} \mu_e N_D \frac{W}{L} \left[ \frac{1000 \text{nm} - 104 \text{nm}}{V_{DS}} \right] \times 10^{-7} \times V_{DS}
\]
Problem 3 - (40 points)

A transfer gate is a circuit designed to move data from one point in a circuit to another, say from Node A to Node B, under the control of a clock signal. A simple MOS transfer gate is shown below. In this circuit, the n-channel MOSFET has $V_T = 0.5$ V independent of $v_{GB}$ and $K = 0.04$ mA/V$^2$. $C_L$ is 45 fF ($= 4.5 \times 10^{-14}$ F).

![Diagram of a transfer gate]

a) [10 points] On the axes provided below, sketch $v_B(t)$ from $t = 0$ to $t = 6T$ when $v_A(t)$ and $v_{CLOCK}(t)$ are as shown. Assume $T$ is much larger than the any charging or discharging transients. (Hints: Treat the terminal, A or B, at the lower potential as the source. Ignore the backgate contact. Node B may not reach 2 Volts.)

![Graphs of $v_A(t)$ and $v_{CLOCK}(t)$]

b) [6 points] What is the average static power dissipated in this transfer gate?

\[
\begin{align*}
\text{No DC current} & \Rightarrow 0 \\
\text{Power Static} & \Rightarrow 0 \\
\text{W}
\end{align*}
\]

Problem 3 continues on the next page.
Problem 3 continued

c) [6 points] What is the energy dissipated during the period from \( t = 0 \) to \( t = 6T \) for the signal sequence you plotted above in Part a?

\[
C_L V^2 = \frac{1}{2} \times 10^{-14} \times (0.5) \times 10 \times 10^{-14}
\]

Energy = \( 10^{-13} \) Joules (W-s)

d) i) [6 points] What is the initial current charging Node B at \( t = T \) in the sequence above?

\[
MOSFET \quad s \uparrow \quad V_G = 2V, \quad V_G - V_T = 1.5V
\]

\[
i = \frac{V}{2} (V_G - V_T) \approx \frac{0.04}{2} (2.25) \times 10^{-5} \quad \text{mA}
\]

Initial charging current = \( 4.5 \times 10^{-5} \) A

ii) [6 points] If this current was maintained constant until the load was charged, how long would it take to charge the output to 2 V? (This doesn't happen, but suppose it did.)

\[
\Delta t = \frac{C_L \Delta V}{I} = \frac{4.5 \times 10^{-14} \times 2}{4.5 \times 10^{-5}}
\]

Charging time = \( 2 \times 10^{-9} \) s

A better MOS transfer gate can be made by adding a p-channel MOSFET driven by a complementary clock signal, as shown at the top of the next page. For this p-channel MOSFET, \( V_T = -0.5 \) V independent of \( V_{GD} \) and \( K = 0.1 \) mA/V².

![MOSFET Diagram]

e) [6 points] Sketch \( v_B(t) \) with the new transfer gate for the same \( v_A(t) \) and \( v_{CLK}(t) \) as above in Part (a).

 ![vB(t) Diagram]

Now reaches 2 V

End of Problem 3
This problem concerns the design of the differential amplifier circuit pictured below. The transistors, $Q_1$, are identical npn bipolar transistors with $\beta = 100$, $v_{BE,ON} = 0.6$ V, $v_{CESAT} = 0.2$ V, and an Early voltage of 50 V. The 2 mA biasing current source is ideal and has infinite output resistance.

![Differential Amplifier Circuit Diagram]

a) [6 points] What are the difference-mode and common-mode input signals to this amplifier when, as shown, $v_{i1} = v_{in}$ and $v_{i2} = 0$? Give your answers in terms of $v_{in}$.

\[
\begin{align*}
    v_{ID} &= \frac{v_{in}}{2} \\
    v_{IC} &= \frac{v_{in}}{2}
\end{align*}
\]

b) [4 points] What value of $R_1$ will yield a quiescent output voltage of 0 V?

\[ R_1 = \frac{1.9}{K} \text{ Ohms} \]

c) [4 points] What is the maximum common-mode input voltage, $v_{IC}$, that can be applied to this amplifier without affecting its operation?

\[ v_{IC,MAX} = \frac{1}{2} \text{ Volts} \]
Problem 4 continued

d) [10 points] In the space below draw a small-signal linear equivalent circuit for the input stage suitable for calculating the difference-mode voltage gain. You may assume that this stage can be analyzed using half-circuit techniques, and use them in your analysis. Clearly label the values of $r_x, g_m, g_o,$ etc.

\[ V_{CC} \]
\[ R_1 \]
\[ g_m \]
\[ r_o \]
\[ R_L \]

\[ R_T = \frac{\beta}{g_m} = \frac{\beta kT}{q I_C} = \frac{100}{10 \times 10^{-3}} = 10 \times 10^3 \Omega = 10 \text{ k}\Omega \]

\[ g_m = \frac{q I_C}{kT} = 10^{-3} \times 10 = 0.1 \text{ mS} \]

\[ g_o = \frac{I_C}{V_A} = \frac{10^{-3}}{50} = 2 \times 10^{-5} \text{ mS} \]

\[ r_o = \frac{1}{2 \times 10^{-5}} = 5 \times 10^4 \Omega = 5 \text{ k}\Omega \]


e) [4 points] Derive an expression for the small signal voltage at the output of the first stage, i.e., $v_m$ when the inputs are those shown, i.e., $v_1 = v_{in}$ and $v_2 = 0$. Note that the common-mode gain is zero when the biasing current source is ideal.

\[ A_{V1} = \frac{v_m}{v_{in} + v_o} \]

\[ A_{vd} = \frac{g_m}{(g_m + g_o + g_L)} \]

f) [12 points] You are asked to design the output stage so that it can deliver ±1 V (about the quiescent value, $V_{OUT}$ of 0 V) to a 1 kOhm load.

i) What is the minimum quiescent collector current that $Q_2$ can have for this design to be met?

\[ I_{CQ2,MIN} = \frac{10^{-3}}{10^{-3}} \text{ Amps} \]

ii) Select $R_2$ to bias $Q_2$ at the level you determined in Part f) i).

\[ R_2 = 3300 \text{ Ohms} \]

iii) What is the quiescent power dissipation in the circuit you have designed?

\[ P_{AVE} = \frac{16 \times 10^{-3}}{16 \times 10^{-3}} \text{ Watts} \]

End of Problem 4
c) [4 points] What is the average DC power dissipation in this circuit?

\[ P_{\text{ave}} = 2 \text{ milliWatts} \]

For the rest of this question use the small signal linear equivalent circuit models below for the transistors in this circuit. Notice that the output conductance is negligible for both devices. Also, use \( C_{gs} = 10 \) fF and \( C_{gd} = 3 \) fF for both devices.

![n-channel MOSFET](image)

\[ g_m V_{gs} \]

\[ C_{gs} \]

\[ C_{gd} \]

\[ v_{gs} \]

\[ d \]

\[ g \]

\[ s \]

\[ + \]

\[ - \]

\[ \text{n-channel MOSFET} \]

![p-channel MOSFET](image)

\[ g_m V_{gs} \]

\[ C_{gs} \]

\[ C_{gd} \]

\[ v_{gs} \]

\[ d \]

\[ g \]

\[ s \]

\[ \text{p-channel MOSFET} \]

d) [9 points] In the space provided below draw the small signal linear equivalent circuit for this amplifier valid at mid-band and at higher frequencies, i.e., when the biasing capacitors (the \( C_{bc} \)'s) are short circuits, but the gate-to-source and gate-to-drain capacitances in the MOSFETs can no longer always be treated as open circuits. Do not reduce your circuit to a two-port here (that is the next part of the question). Provide numerical values for the transconductances and calculate the mid-band voltage gain.

\[ g_m (\text{n-channel}): 2 \times 10^{-3} \]  

\[ g_m (\text{p-channel}): 1 \times 10^{-3} \]

\[ A_v = \frac{v_{out}}{v_{in}} \cdot \frac{(5k)}{12+5k} \cdot \left( \frac{1}{g_m} \right) \cdot 10k \]

\[ A_v = -5 \text{ (30)} \approx -2 \]
e) [8 points] Find $r_{in}$, $C_{in}$, $A_{v,oc}$, and $r_{out}$ for the approximate two-port equivalent circuit shown below for your circuit in Part d) above.

\[ C_{in} = 20f + (1 + 30) f \]
\[ = 206 f \]
\[ r_{in} = 5 \text{ K Ohms} \]
\[ C_{in} = \frac{206}{f} \text{ Farads} \]
\[ A_v = \frac{3 \times 10^{-3}}{10k} = -30 \]
\[ r_{out} = 10 \text{ K Ohms} \]

f) [4 points] Provide an expression for an estimate of the high frequency breakpoint, $\omega_{hi}$, of this amplifier using the open circuit time constant method. If you could not do Part e) above, express your answer in terms of the two-port parameters.

\[ T_1 = C_{in} \left( r_{in} H R_f \right) = 20f \left( 5 \times 111k \right) = 20f \left( 833k \right) \]
\[ = 0.172 \text{ ns} = 172 \text{ ps} \]
\[ T_L = C_{L} \times R_{out} = 30f \times 100k = 3000f \]
\[ T_1 + T_L = 472 \text{ ps} \]
\[ \omega_{hi} = \frac{2.12 \times 10^9}{\text{Radians/s}} \]

End of Problem 5

End of Exam

Happy Holidays; have a great IAP
Problem 5 - (40 points)

This problem concerns the circuit shown below. For the n-channel MOSFET K is 8.0 mA/V² and \( V_T \) is 0.5 V; for the p-channel MOSFETs K is 2.0 mA/V² and \( V_T \) is -0.5 V.

![Diagram of the circuit](image)

a) [6 points] Compute the DC bias currents \( I_1 \) and \( I_2 \).

\[
I_1: \quad \frac{2}{3} F \quad \text{mA}
\]

\[
I_2: \quad \frac{2}{3} F \quad \text{mA}
\]

b) [9 points] Compute the DC bias voltages at nodes A, B, and C.

\[
\begin{align*}
    \sum V_{\text{in}} - V_T &= \sqrt{2 \left( \frac{I_0}{K} \right)^2} \\
    &= \sqrt{2 \left( \frac{2 \times 1.2 \times 10^{-3}}{8 \times 10^{-3}} \right)^2} \approx \sqrt{\frac{1}{16}} \approx \frac{1}{4}
\end{align*}
\]

At node A: \( \frac{2}{3} F + \frac{1}{3} F = \frac{7}{3} F \) Volts

At node B: \( \frac{7}{3} F + \frac{1}{3} F = \frac{8}{3} F \) Volts

At node C: \( \frac{7}{3} F \) Volts

Problem 5 continues on the next page.