Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology

6.012 Electronic Devices and Circuits

FINAL EXAMINATION

Thursday, May 18, 2000
Johnson Athletic Center, 1:30 pm to 4:30 pm
Open book.

Notes:

1. Unless otherwise indicated, assume room temperature and that \( kT/q \) is 0.025 V, \( kT/q \ln 10 = 60 \text{ mV} \), and \( n_i = 10^{10} \text{ cm}^{-3} \) for Si.

2. This test is designed so that most parts can be worked independently of the others.

3. All of your answers and any relevant work must appear on these pages. Any additional paper you hand in will not be graded.

4. Make reasonable approximations and assumptions. State and justify any such assumptions and approximations.

5. Be certain that you have all twelve (12) pages of this exam booklet and make certain that you write your name at the top of this page as indicated.

6. You may see your final exam in Room 13-3058 beginning June 5, 2000.

Grader Use Only

PROBLEM 1

PROBLEM 2

PROBLEM 3

PROBLEM 4

TOTAL

(out of 20 possible)

(out of 25 possible)

(out of 28 possible)

(out of 27 possible)
Problem 1 - (20 points)

Warm-up questions:

a) A sample of silicon is known to contain $10^{17}$ cm$^{-3}$ arsenic atoms (column V) and $5 \times 10^{16}$ cm$^{-3}$ boron atoms (column III). What are the thermal equilibrium hole and electron concentrations in this sample at room temperature where $n_i = 10^{10}$ cm$^{-3}$?

$$n_o = \frac{5 \times 10^{16}}{\text{cm}^3} + 2$$

$$p_o = \frac{2000}{\text{cm}^3} + 2$$

b) A high quality long base silicon p-n diode is inadvertently irradiated in a nuclear reactor with the consequence that the minority carrier lifetimes on the n- and p-sides decrease from $10^{-4}$ s to $10^{-8}$ s (no other materials parameters change). How much, if at all, does the diode saturation current change?

$$\frac{I_{ES(\text{after})}}{I_{ES(\text{before})}} = 100 + 4$$

c) i) Rank order the common-emitter (CE), common-base (CB), emitter follower (EF) bipolar linear amplifier configurations in order of increasing input resistance, assuming comparable bias levels, $I_C$:

- CB
  Lowest
- CE
  Middle
- EF
  Highest

Explanations:

ii) Rank order the common-source (CS), common-gate (CG), source follower (SF) MOSFET linear amplifier configurations in order of increasing output resistance, assuming comparable bias levels, $I_D$:

- SF
  Lowest
- CS
  Middle
- CG
  Highest

Explanations:

Problem 1 continues on the next page.
Problem 1 continued

d) Answer in five words or less:

i) CMOS is one of the fastest MOSFET logic families and it is used in the highest speed microprocessors. At the same time, one of the most important applications for CMOS is in low speed circuitry. What is CMOS's advantage for low speed applications?

\[ \text{no static power dissipation} \quad +2 \]

ii) What major structural change was made to enable the 486 to run faster than the 386 (and again to make the Pentium faster than the 486)?

\[ \text{Smaller devices} \quad (L \to \frac{1}{2}) \quad +1 \]

iii) Why is CMOS attractive for linear amplifier applications? Give one reason (there are several).

\[ \text{infinite input resistance} \quad +1 \]

\[ \text{high gain} \]

e) A certain common-emitter bipolar transistor amplifier is fabricated using resistors whose resistance is insensitive to temperature and with transistors whose forward current gain, $\beta_F$, Early voltage, $V_A$, and base-emitter knee voltage, $V_{BE,ON}$, are essentially unchanged between room temperature (25°C) and 100°C. None the less, when this amplifier is heated to 100°C its voltage gain, $A_v$, drops noticeably. Give an explanation as to why the voltage gain might change and use your explanation to estimate $A_v(100°C)/A_v(25°C)$.

\[ T = 300 \to 375 \]

\[ G_m = \frac{I_c}{kT/Q} \quad \text{Ic Unchanged,} \quad \frac{kT}{Q} \quad +4 \]

\[ A_v(100°C)/A_v(25°C) \approx 0.8 \]

End of Problem 1
Problem 2 - (25 points)

The symmetric p-n diode shown below, with \( N_{Ap} = N_{Nn} = 10^{16} \text{ cm}^{-3} \), is illuminated by steady state light that generates \( M \) hole-electron pairs/cm\(^2\)-s uniformly over the plane at \( x = 2w_n/3 \). The p- and n-region widths, \( w_n \) and \( w_p \), are both 5 \( \mu \text{m} \), and both minority carrier diffusion lengths are much larger than this, i.e., \( L_e, L_h > 6 \mu \text{m} \). The electron mobility, \( \mu_e \), is 1600 cm\(^2\)/V-s, and the hole mobility, \( \mu_h \), is 600 cm\(^2\)/V-s. Neglect the depletion region widths relative to 6 \( \mu \text{m} \).

\[ n'(x), p'(x) \]

\[ \frac{n_i^2}{N_A} \left( e^{\frac{\alpha}{kT} V_{AB}} - 1 \right) = \begin{cases} 2.4 \times 10^{13} \text{ cm}^{-3} & kT = 0.02 \\ 1.0 \times 10^{13} \text{ cm}^{-3} & kT = 0.021 \end{cases} \]

a) On the axes below plot the excess minority carrier concentrations throughout the diode when \( V_{AB} = 0.54 \text{ V} \) and \( M = 0 \).

b) If we take as the criterion for low level injection (LLI) that the excess minority carrier concentration must not exceed 10% of the equilibrium majority carrier concentration, how large can \( V_{AB} \) be before LLI is violated when \( M = 0 \)?

\[ V_{AB} = \frac{kT}{q} \ln \left( \frac{n_{\text{MAX}} N_A}{n_i^2} \right), \quad n_{\text{MAX}} = \frac{N_A}{10} \]

\[ V_{AB} \leq \begin{cases} 0.66 \text{ V} & kT = 0.025 \\ 0.63 \text{ V} & kT = 0.025 \end{cases} \]

c) Now consider setting \( V_{AB} = 0 \), i.e., short circuiting the diode, and applying illumination, \( M = 3.75 \times 10^{13} \text{ cm}^{-2}\text{s}^{-1} \). On the axes provided at the top of the next page plot the excess minority carrier concentrations throughout the diode now. Assume \( p' \) has the value indicated on the axes at \( x = 2w_n/3 \).

Problem 2 continues on the next page.
d) On the axes below make labeled plots of the hole current density, $j_H$; the electron current density, $j_E$; and the total current density, $j_{TOTAL}$; throughout the short-circuited, illuminated device.

i) Hole current density:

\[ j_H = \frac{2}{3} q M = 4 \frac{\mu A}{cm^2} \]

ii) Electron current density:

\[ j_E = -2 \frac{\mu A}{cm^2} \]

iii) Total current density:

\[ j_{TOTAL} = - \frac{1}{3} q M = -2 \frac{\mu A}{cm^2} \]

Problem 3 continues on the next page.
Problem 2 continued

e) i) What is \( p'(2w_n/3) \)?

\[
p'(\frac{2w_n}{3}) = \frac{2}{9} \frac{M W_n}{D_n}
\]

\[
p'(2w_n/3) = 3.33 \times 10^8 \text{ cm}^{-3}
\]

ii) How large can \( M \) be before LLI is violated when \( V_{AB} = 0 \)?

\[
p'(\frac{2w_n}{3}) \leq \frac{N_A}{10}
\]

\[
M \leq \frac{N_A}{10} \frac{9}{2} \frac{D_n}{M W_n}
\]

\[
M \leq 1.12 \times 10^{20} \frac{1}{\text{cm}^2 \text{s}}
\]

End of Problem 2
Problem 3 - (28 points)

Consider the two silicon device structures shown in cross-section below:

Device A:

Device B:

Both of these devices are made on p-type silicon with a net doping level of $10^{17}$ cm$^{-3}$, and are 20 μm wide normal to the page. The n+ regions are doped to $10^{18}$ cm$^{-3}$, and the n+-p junction is 1 μm from the top surface. The thin oxide is a high quality thermal oxide 16 nm thick, and covers an area 20 μm wide by 15 μm long. In Device A the n+ region is 20 μm wide by 5 μm long and extends just up to the edge of the thin oxide, while in Device B it is 20 μm wide by 20 μm long and extends all the way under the thin oxide, as shown in the figure.

You may assume that throughout the silicon the electron mobility, $\mu_e$, is 1600 cm$^2$/V-s and the hole mobility, $\mu_h$, is 600 cm$^2$/V-s (except in an inversion layer in which case $\mu_e = 600$ cm$^2$/V-s and $\mu_h = 400$ cm$^2$/V-s); that the intrinsic carrier concentration, $n_i$, is $10^{10}$ cm$^{-3}$ at room temperature; and that the dielectric constant, $\varepsilon_{Si}$, is $10^{-12}$ F/cm. The dielectric constant of the oxide, $\varepsilon_{ox}$, is $3 \times 10^{-13}$ F/cm, and the electrostatic potential of the gate metal relative to intrinsic Si is 0.3 V.

a) i) What is the electrostatic potential of the p-type silicon, relative to intrinsic silicon, in thermal equilibrium at room temperature?

$$\Phi_p = -\frac{kT}{q} \ln \frac{N_A}{n_i}$$

Electrostatic potential = $-0.4$ V

ii) What is the built-in potential of the unbiased n+-p junction at room temperature?

$$\Phi_b = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2}$$

Built-in potential = 0.86 V

Problem 3 continues on the next page.
b) What are the flat band voltages, \( V_{FB} \), of the MOS capacitor structures in Devices A and B, respectively?

\[
V_{FBA} = \phi_{MSA} - \phi_{n+} = -0.3\ V - 0.4\ V = -0.7\ V
\]

\[
V_{FBB} = \phi_{MSA} + \phi_{n+} = -0.3\ V + 0.46\ V = +0.16\ V
\]

\( V_{FB} \) (Device A) = \(-0.7\ V\)  \( V_{FB} \) (Device B) = \(+0.16\ V\)

c) The magnitude of the threshold voltage, \(|V_T|\), for the MOS structure is 1 V in one of these devices, and 4 V in the other. Use this information and your knowledge of MOS capacitors to deduce the magnitude and sign of \( V_T \) for each of these MOS capacitors, i.e., the one made on p-Si and the made on n+Si.

\[
V_T = V_{FB} + \frac{2q\varepsilon\varepsilon_0 N_A}{C_{ox}} \sqrt{2}\phi
\]

\( V_{TA} = 0.88\ V \)

\( V_{TB} = 3.40\ V \)

\( V_T \) (Device A) = \(+1\ V\)  \( V_T \) (Device B) = \(-4\ V\)

d) What is the condition (accumulated, depleted, or inverted) of the semiconductor surface under the thin oxide in each of these devices with a gate voltage, \( V_{GB} \), of 2 Volts? Also give the identity and sheet density of any mobile holes or electrons induced at the oxide-silicon interface.

Device A:

\[
\frac{Q}{q} = \frac{C_{ox}}{q} (V_{GB} - V_{TA}) = \frac{V_T = 1\ V}{1.3 \times 10^{12}\ cm^{-2}}
\]

Surface condition: INVERTED

Carrier type and sheet concentration: electrons

Device B:

\[
\frac{Q}{q} = \frac{C_{ox}}{q} (V_{GB} - V_{FB})
\]

Surface condition: ACCUMULATED

Carrier type and concentration: electrons \( 2.4 \times 10^{12}\ cm^{-2} \)

Problem 3 continues on the next page
Problem 3 continued

Next consider using these devices as the storage capacitor in the dynamic memory cell illustrated below. The MOSFET is an n-channel device with a threshold voltage, $V_T$, of 0.75 V (ignor any variation with $v_{BS}$) and a drain current in saturation of $0.1 \ (v_{GS} - V_T)^2 \ mA$.

![Diagram of MOSFET circuit]

c) If $V_{GB}$ is initially 0 V and $V_{AB}$ is increased from 0 V to 2 V, what will the new value of $V_{GB}$ be?

$$V_{GB} = V_{AB} - V_{Tmos} = 2 - 0.75 = 1.25 \ V$$

f) After having been 2 V for a long period of time, $V_{AB}$ is switched to 0 V at $t = 0$. How will $V_{GB}$ vary with time for $t > 0$? Give its initial value and describe how it changes with time, if at all.

* No discharge if we ignore the n+p diode connected to G.
* If we include the reverse bias leakage of the diode, then there will be a very slow discharge with fixed slope $\frac{dv_{GB}}{dt} = -1.25$ V.

End of Problem 3
Consider the differential amplifier circuit illustrated below:

In this circuit the three n-channel MOSFETs are identical; they have a threshold voltage, $V_T$, of 1 V, a drain current in saturation of $2.5(v_{GS} - V_T)^2$ mA, and an Early voltage of 10 V. The npn bipolar junction transistors (BJTs) have forward betas, $\beta_F$, of 100 and reverse betas, $\beta_R$, of 5; and base-emitter saturation currents, $I_{ES}$, of $10^{-12}$ A; unless otherwise indicated you may use $|V_{BE,ON}| = 0.6$ V; $|V_{CE,SAT}| = 0.2$ V. The Early voltage of the npn's is 50 V. The MOSFETS do not operate properly if $(v_{GS} - V_T)$ is less than 0.2 V. Assume $C_S$ is a short in mid-band.

Note that value of the resistor $R_4$, the quiescent collector current on $Q_4$, and minimum quiescent voltage on the gate of $Q_3$ are indicated on the schematic, as are the supply voltages.

a) What must the bias level ($I_{Bias}$) on $Q_3$ be to have a quiescent output voltage of approximately 0 V? (Assume that the quiescent collector current of $Q_4$ is 2 mA, as indicated, and do not forget its base current.)

\[ \frac{1.4V + 0.02}{6.4k\Omega} \leq 0.2mA \]

\[ I_{Bias} = \frac{0.2mA}{mA} \]

Problem 4 continues on the next page
Problem 4 continued

b) Select $R_5$ be to be consistent with a quiescent collector current in $Q_4$ of 2 mA, and a quiescent output voltage of approximately 0 V.

\[
\text{Need } 2mA \times R_5 = 2V \Rightarrow R_5 = \frac{1000}{990} \text{ (or } 990) \Omega
\]

\[R_5 = \frac{1000}{990} \Omega\]

c) Select $R_1$ to give a bias current through $Q_5$ of 1 mA. You may ignore the base currents of $Q_5$, $Q_6$, and $Q_7$.

\[4 - 0.6 = \frac{3.4V}{3.4mA} = 1 \Omega
\]

\[R_1 = \frac{3400}{\Omega}\]

d) i) In the space below sketch a small signal linear equivalent circuit one could use to calculate the signal voltage on the gate of $Q_3$ due to the differential-mode input signal, $v_{in1} - v_{in2}$. Find an expression for this voltage in terms of incremental linear equivalent circuit model parameters.

\[
\text{Sketch of small signal equivalent circuit}
\]

\[V_{out} = g_{m2}R_3 \frac{V_{in}}{2}\]

ii) Determine how the differential-mode voltage gain of the differential stage ($Q_1$ and $Q_2$) varies with the quiescent drain current of $Q_1$ and $Q_2$, and find the maximum differential-mode voltage gain (magnitude), the corresponding "optimum" drain bias current, $I_{D,\text{opt}}$, and value for $R_{2,\text{opt}}$ ($= R_{3,\text{opt}}$).

\[
g_m = \sqrt{2KI_0} \quad A_{vd} = \frac{V_{out}}{V_{in}} = \frac{g_{m2}R_3}{2} = \frac{\sqrt{2KI_0}R_3}{2}
\]

\[= \sqrt{\frac{K}{2I_0}} \cdot I_0 R_3 \quad \Rightarrow \frac{I_0 R_3}{(V_{GS} - V_T)} < \frac{2}{0.2} \approx 10\]

\[|A_{vd,\text{max}}| = \frac{10}{0.1} \quad I_{D,\text{opt}} = 0.1 \text{ mA} \quad R_{2,\text{opt}} = \frac{20000}{\Omega}
\]

\[V_{GS} - V_T = 0.2 \quad \Rightarrow I_D = 2.5 \times (0.2)^2 = 0.1 \text{ mA} \quad I_D R_3 = 2V \Rightarrow R_3 = \frac{2}{0.1} = 20 \Omega
\]

Problem 4 continues on the next page
e) Suppose you can replace $R_2$ and $R_3$ with a current mirror made with p-channel MOSFETs with $|V_T| = 1$ V and $|V_A| = 20$ V. In the space below draw the schematic of such a current mirror, and discuss what impact this would have on the voltage gain.

f) Looking at the output stage, what are the most positive and negative values of $V_{out}$ possible?

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End of Problem 4 and the Exam.

Because $C_3$ is one, $V = 6.4$ can't be a static, voltage divider and $5.5$.

Accept assuming limit is $AV$ across $R_V = 0$. 