Lecture 14 - **Digital Circuits: Inverter Basics** - Outline

- **Announcements**
  - Handout - Lecture Foils; two supplemental readings on Stellar
  - The MOSFET alpha factor - use definition in lecture, not text

- **Review** - Adding refinements to large signal models
  - **Charge stores**: depletion regions, excess carriers, gate charge
  - **Active-length modulation**: the Early effect
  - **Extrinsic parasitics**: Lead resistances, capacitances, and inductances

- **Digital building blocks - inverters**
  - A generic inverter
  - MOS inverter options

- **Digital inverter performance metrics**
  - **Transfer characteristic**: logic levels and noise margins
  - **Power dissipation**
  - **Switching speed**
  - **Fan-out, fan-in**
  - **Manufacturability**

- **Comparing the MOS options**
  - And the winner is….
**Charge stores in devices:** we must add them to our device models

**Parallel plate capacitor**

\[ q_{A,PP} = A \frac{\epsilon}{d} v_{AB} \]

\[ C_{pp}(V_{AB}) = \left. \frac{\partial q_{A,PP}}{\partial V_{AB}} \right|_{V_{AB}=V_{AB}} = A \frac{\epsilon}{d} \]

**Depletion region charge store**

\[ q_{A,DP}(V_{AB}) = -A \sqrt{2q\epsilon_{Si} \left[ \phi_b - v_{AB} \right]} \frac{N_{Ap}N_{Dn}}{N_{Ap} + N_{Dn}} \]

\[ C_{dp}(V_{AB}) = A \sqrt{\frac{q\epsilon_{Si}}{2[\phi_b - V_{AB}]} \frac{N_{Ap}N_{Dn}}{N_{Ap} + N_{Dn}}} = \frac{A \epsilon_{Si}}{w(V_{AB})} \]

**QNR region diffusion charge store**

\[ q_{AB,DF}(V_{AB}) \approx A q n_i^2 \frac{D_h}{N_{Dn}w_{n,eff}} \left[ e^{qV_{AB}/kT} - 1 \right] \]

\[ C_{df}(V_{AB}) \approx \frac{w_{n,eff}^2}{2D_h} \frac{q I_D(V_{AB})}{kT} \]

*Note: Approximate because we are only accounting for the charge store on the lightly doped side.*
Adding charge stores to the large signal models:

**p-n diode:**

- **q_{AB}**: Excess carriers on p-side plus excess carriers on n-side plus junction depletion charge.

**BJT:** npn (in F.A.R.)

- **q_{BE}**: Excess carriers in base plus E-B junction depletion charge
- **q_{BC}**: C-B junction depletion charge

**MOSFET:** n-channel

- **q_{G}**: Gate charge; a function of \( v_{GS} \), \( v_{DS} \), and \( v_{BS} \).
- **q_{DB}**: D-B junction depletion charge
- **q_{SB}**: S-B junction depletion charge
The Early Effect: (exaggerated for impact)

BJT: npn

\[-\frac{1}{\lambda} = -V_A\]

MOSFET: n-channel

\[-\frac{1}{\lambda} = -V_A\]
Output Characteristics

**BJT:** npn

\[ i_C \approx \beta_F (1 + \lambda V_{CE}) i_B \]

**MOSFET:** n-channel

\[ i_D \approx K [v_{GS} - V_T(v_{BS}) - v_{DS}/2] v_{DS} \]

\[ i_D \approx K [v_{GS} - V_T(v_{BS})]^2 [1 + \lambda (v_{DS} - V_{DSat})/2] \]
Large signal models: when will we use them?

Digital circuit analysis/design:
This requires use of the entire circuit, and will be the topic of this and the next lecture (Lecs. 14 and 15).

Bias point analysis/design:
This uses the FAR models (Lec. 17ff).

![BJT Diagram](image)

![MOSFET Diagram](image)
Large Signal Characteristics of MOSFETs and BJTs:
Models used for initial hand calculations of transfer characteristics

MOSFET

\[ i_D = \beta_F i_B \]

\[ v_D = 0 \]

\[ v_B = 0 \]

\[ i_G \approx 0 \]

\[ v_{GS}, v_{DS}, v_{BS} \]

\[ i_D(v_{GS}, v_{DS}, v_{BS}) \]

\[ v_{DS} \geq 0 \]

\[ v_{BS} \leq 0 \]

\[ i_B \approx 0 \]

\[ i_G \approx 0 \]

\[ i_D \approx 0 \]

\[ i_D \approx K(v_{GS} - V_T - v_{DS}/2)v_{DS} \]

BJT

\[ \beta_F i_B \]

\[ v_{BE}, v_{BE,ON} \]

\[ v_{BE} \]

\[ v_{CE, sat} \approx 0.2 V \]

\[ v_{CE} \]

\[ i_C \approx \beta_F i_B \]

\[ i_C \approx 0 \]

\[ \alpha = 1 \]

\[ v_A = \infty \]
MOSFET Circuit symbols: an aside about different symbols used for MOSFETS in schematic circuit drawings

**n-channel**

- Linear schematics
- Enhancement mode
- Digital schematics
- Depletion mode

**p-channel**

(usual circuit orientation)

- Linear schematics
- Enhancement mode
- Digital schematics
- Depletion mode
• Building Blocks for Digital Circuits: **inverters**

A basic inverter

Switch: on or off

Logic gates

NOR:

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<tr>
<th>$v_A$</th>
<th>$v_B$</th>
<th>$v_{OUT}$</th>
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Performance metrics

- Transfer characteristic
- Logic levels
- Noise margins
- Power dissipation
- Switching speed
- Fan-in/Fan-out
- Manufacturability

Memory cell

Flip-flop

Clif Fonstad, 4/4/06
**Transfer characteristic**

Node equation: \( i_{PD} = i_{PU} \)

\[
i_{PD} = \begin{cases} 
0 & \text{when } v_{IN} < V_{T,PD} \\
K_{PD}(v_{IN} - V_{T,PD})^2 / 2 & \text{when } 0 < [v_{IN} - V_{T,PD}] < v_{OUT} \\
K_{PD}(v_{IN} - V_{T,PD} - v_{OUT}/2)v_{OUT} & \text{when } 0 < v_{OUT} < [v_{IN} - V_{T,PD}] 
\end{cases}
\]

\( i_{PU} \): Depends on the specific pull-up device used.

**Switching times**

Charging cycle: \( i_{Charge} = i_{PU} \)

Discharging cycle: \( i_{Discharge} = i_{PD} - i_{PU} \)

**Power**

\[
P_{Total} = P_{Static} + P_{Dynamic}
\]

Static:

\[
P_{Static} = \frac{1}{2} i_{PU, on} V_{DD}
\]

Dynamic:

\[
P_{Dynamic} = C_L V_{DD}^2 \cdot f
\]
MOS inverters: 5 pull-up choices

Generic inverter

- n-channel, e-mode pull-up
  - $V_{DD}$ on gate
  - $V_{GG}$ on gate

- Resistor pull-up

- Active p-channel pull-up (CMOS)

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**Switching transients**

**General approach:**
The load, \( C_L \), is a non-linear charge store, but for MOSFETs it is fairly linear and it is useful to think linear:

\[
dv_{\text{out}}/dt \approx i_{\text{CL}}/C_L
\]

**Bigger current → faster \( v_{\text{OUT}} \) change**

\( \Rightarrow \) **CHARGING \( C_L \):**
The charging current for the various MOSFET pull-up options

**Charging cycle:**
\[
i_{\text{Charge}} = i_{\text{PU}}
\]

**Discharging cycle:**
\[
i_{\text{Discharge}} = i_{\text{PD}} - i_{\text{PU}}
\]
Switching transients, cont.

⇒ DISCHARGING $C_L$:
The discharging current for the various pull-up options

Discharging cycle:

\[ i_{\text{Discharge}} = i_{PD} - i_{PU} \]

- The discharge current ($i_{\text{Discharge}}$) is the difference between the upper curve ($i_{PD}$) and the appropriate lower curve ($i_{PU}$).

Which pull-up is best? To see we can look at each in turn and then compare them.
Switching transients, cont.

Charging and discharging:
Linear resistor pull-up

\[ \text{i}_{\text{PU}} = \text{i}_{\text{Charge}} \]

\[ \text{i}_{\text{PD}} = \text{i}_{\text{Discharge}} + \text{i}_{\text{PU}} \]

Simple
Least costly with discrete components but integrated resistors consume lots of space.

\[ \tau_{\text{Charge}} >> \tau_{\text{Discharge}} \]
Switching transients, cont.

Charging and discharging:
Saturated E-mode pull-up

\[ i_{\text{PU}} = i_{\text{Charge}} \]

\[ i_{\text{PD}} = i_{\text{Discharge}} + i_{\text{PU}} \]

No added cost in adding more MOSFETs
No added wiring
Slower than linear resistors

\[ \tau_{\text{Charge}} \gg \tau_{\text{Discharge}} \]
Switching transients, cont.

Charging and discharging: Linear E-mode pull-up

\[ i_{PU} = i_{Charge} \]

\[ i_{PD} = i_{Discharge} + i_{PU} \]

Still compact
Need to wire VGG to each gate
Need second supply
Not faster than linear resistor

\[ \tau_{Charge} >> \tau_{Discharge} \]
Switching transients, cont.

Charging and discharging:
D-mode pull-up ("nMOS")

Charging and discharging:
D-mode pull-up ("nMOS")

Compact
Symmetrical charge/discharge
Fastest possible
Must make E- and D-mode on safe wafer

\[ i_{PU} = i_{\text{Charge}} \]

\[ i_{PD} = i_{\text{Discharge}} + i_{PU} \]

\[ \tau_{\text{Charge}} \approx \tau_{\text{Discharge}} \]
Switching transients, cont.

Charging and discharging:
Active complementary pull-up ("CMOS")

\[ I_{PD} = I_{Discharge} + I_{PU} \]

Symmetrical charge/discharge
Almost as fast, or even faster than, n-MOS
No static power dissipation \((I_{ON} = 0)\)
Must make n- and p-channel on same wafer

\[ \tau_{Charge} \approx \tau_{Discharge} \]
Switching transients: summary of charge/discharge currents

- Resistor and E-mode pull-up (\(V_{GG}\) on gate)
- E-mode pull-up (\(V_{DD}\) on gate)
- D-mode pull-up (called "n-MOS")
- CMOS

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- Comparisons made with same pull-down MOSFET, load, \(V_{Hi}\), and \(I_{ON}\).
Digital building blocks - inverters

A generic inverter: Switch = pull-down device, Load = pull-up device
MOS inverter options - Pull-down: n-channel, e-mode (faster than p-channel)
   Pull-up: 1. resistor; 2. n-channel, e-mode w. and w.o. gate bias;
            3. n-channel, d-mode; 4. p-channel, e-mode (CMOS)

Digital inverter performance metrics

Transfer characteristic
   Logic levels: \( V_{HI}, V_{LO} \)
   Noise margins: \( NM_{HI} \) (high), and \( NM_{LO} \) (low)
   Design variables: choice of pull-up device
                    pull-up and pull-down thresholds
                    device sizes (absolute and relative)

Power dissipation: stand-by power and switching dissipation
Switching speed: capacitive load
                    charge and discharge currents critical

Fan-out, fan-in: minimal issue in MOS; more so with BJT logic

Manufacturability: small, fast, low-power, reliable, and cheap

Comparing the MOS options

And the winner is… CMOS