6.012 ELECTRONIC DEVICES AND CIRCUITS

Schedule -- Spring 2006 (5/3/06)

Notice:  We made this schedule carefully, but use it only as an indication of what is expected to happen; it will undoubtedly change as we go along.

Lecture 1 -- Tuesday, Feb. 7:  Introduction.  Intrinsic semiconductors, bond structure, holes and electrons; \( n_s(T) \).  Dopants -- donors and acceptors. \( n_o \) and \( p_o \) in extrinsic (doped) Si:  thermal equilibrium, detailed balance, \( n_o p_o \) product; \( n_o \) and \( p_o \) given \( N_A \) and \( N_D \).

Recitation 1 -- Wednesday, Feb. 8:  Calculations of \( n_o \), \( p_o \) in variously doped examples to review "\( n_o \) and \( p_o \) given \( N_A \) and \( N_D \)" from lecture.  Drift, basic concepts:  net velocity vs. field, mobility; conductivity, resistivity.  Concept of n-type and p-type.  Problem Set #1 out (equilibrium carrier concentrations, drift and conductivity, population transients).


Tutorial 1 -- Mon/Tues, Feb. 13/14:  Review of electrostatics (8.02) and Poisson's equation; \( \rho \), \( E \), \( \phi \); parallel plate capacitors.  Doping and carrier type issues as needed.


Lecture 4 -- Thursday, Feb. 16: Linearization and decoupling of 5 basic equations in flow problem regime: quasineutrality, Debye length, \( L_{Dx} \), and dielectric relaxation time, \( \tau_D \); minority carrier flow by diffusion. Diffusion equation(s) for \( n' \): general solutions; boundary conditions; procedure to find \( n \), \( p \), \( J_x \), \( J_n \), \( E_x \), \( E_n \) having \( n' \).

Recitation 4 -- Friday, Feb. 17: Boundary conditions for flow problems: ohmic contacts, reflecting surfaces, continuity at internal boundaries.  Example of injection in middle of a bar; short-base and long-base limits.

Tutorial 2 -- Tues\(^1\), Feb. 21: Population transient problems. Identification of simple situations as special cases of the five basic equations.

Recitation 5 -- Wednesday, Feb. 22: More (final) discussion and solutions of flow problems as needed.  Integral solutions in long diffusion length (infinite lifetime) limit. Problem Set #3 out (electrostatic potential; electrostatics of abrupt p-n junctions, depletion capacitance).

Lecture 5 -- Thursday, Feb. 23: Non-uniformly doped material in thermal equilibrium. Electrostatic potential (using Einstein relation); Poisson equation. \( n_o(x) \), \( p_o(x) \), \( \phi(x) \) when doping varies slowly; quasi-neutral approximation; mention of extrinsic Debye length, \( L_x \). Problem Set #2 due.

\(^1\) Monday, Feb. 20 is a holiday and there are no tutorials. All students should attend the tutorial of their choice on Tuesday, Feb. 21.
Recitation 6 -- Friday, Feb. 24: Review concepts in Lecture 5. Discussion of electrostatic potential energy, $q\phi$. Typical values of $\phi_n$, $\phi_o$, emphasize weak dependence on $n_o$, $p_o$; 60 mV/decade rule. Look $n_o$, $p_o$, and $\phi$’s in vicinity of an abrupt p-n junction.

Tutorial 3 -- Mon/Tues. Feb. 27: More (final) discussion of flow problems, boundary conditions, and solutions. Estimation of recombination under profile obtained assuming infinite lifetime. Electrostatic potential of various metals and semiconductors, and consideration of $\phi(x)$ around a circuit and through contacts in T.E.

Lecture 6 -- Tuesday, Feb. 28: Abrupt p-n junction in thermal equilibrium; the depletion approximation. Expressions for $W$, $x_n$, $x_p$, $E_{plk}$, $\phi_b$. Extension of model to biased junctions: argue can replace $\phi_b$ by ($\phi_b$ - $v_A$) if charge due to currents can be neglected and all $v_A$ appears across junction.

Recitation 7 -- Wednesday, March 1: Review depletion approximation model for junction and the effect of bias; comment on $\phi(x)$ around a circuit through contacts (Note: was done in tutorials). Charge store associated with SCL and depletion capacitance. *Problem Set #3 due; Problem Set #4 out (current flow in p-n diodes; diffusion capacitance).*

Lecture 7 -- Thursday, March 2: Forward biased abrupt p-n junction. Carrier equilibrium with/across space charge layer; current flow. Derivation of I-V expression. Plots of carrier populations through forward and reverse biased short base p-n diodes (emphasize injection is into lightly doped side).

Recitation 8 -- Friday, March 3: Charge storage associated with minority carrier injection; diffusion capacitance

Tutorial 4 -- Mon/Tues, March 6/7: Examples of various junction profiles (p-i-n, p-n-n+, etc.) to re-enforce understanding of the depletion approximation and the electrostatics of p-n junctions.

Lecture 8 -- Tuesday, March 7: Review diodes current, and QN region exceed charge stores and diffusion capacitance; introduce BJT structure, and bipolar junction transistor (BJT) operating principles; derive currents for npn BJT in forward active region; introduce base and emitter defects.

Recitation 9 -- Wednesday, March 8: Review of BJT issues, focusing on reverse biased CB diode and impact of carrier injection toward it. Schematic symbols for BJTs and example inverter/amplifier circuits; compare to MOSFET from 6.002; discuss two viewpoints: base-emitter voltage and base current as controlling collector current. *Problem Set #4 due; Problem Set #5 out (BJT modeling; Ebers-Moll; applying BJT models; photodetectors).*

Lecture 9 -- Thursday, March 9: Superposition, Ebers-Moll model for npn. Expressions for $\alpha$ and $\beta$. Large signal BJT characteristics and models: regions of operation; approximate model valid in forward active region. $\beta$-model. Discussion of limitations of model and extremes of operation; non-ideal elements

Recitation 10 -- Friday, March 10: Complete discussion of large signal BJT models. Use large signal BJT model to calculate transfer characteristic of common emitter amplifier.

Tutorial 5 -- Mon/Tues, March 13/14: Plots of carrier populations and current densities through BJTs in various operating regions. Review of material to date in preparation for first exam.

Lecture 10 -- Tuesday, March 14: Other junction devices (a disguised quiz review): LEDs, illuminated p-n diodes; superposition; solar cells and photodiodes.
**Review 1** -- Wednesday, March 15: No formal recitation sessions. Instructors will be available to answer questions and review issues for the quiz.

**Quiz 1** -- Wednesday, March 15, 7:30 to 9:30 pm, Rm 50-340 (Walker Memorial). Closed book. Covering material through 3/3/06 and Problem Set #4 (i.e., through p-n diodes).

**Lecture 11** -- Thursday, March 16: MOS structures. Discussion of accumulation, depletion, inversion. Application of depletion approximation to MOS capacitor to relate channel charges to gate voltage. Flat band voltage; threshold voltage.

**Recitation 11** -- Friday, March 17: Review accumulation, depletion, and inversion in MOS, and model relating channel charge to gate voltage in excess of threshold. C-V relationship for MOS structure. *Problem Set #5 due; Problem Set #6 out (MOS capacitor; MOSFET modeling).*

**Tutorial 6** -- Mon/Tues, March 20/21: Discussion of MOS structure and MOS capacitor issues.

**Lecture 12** -- Tuesday, March 21: Gradual channel approximation for MOSFET i-v characteristics; quadratic approx. Discussion of pinch-off. Regions of operation.

**Recitation 12** -- Wednesday, March 22: Review of gradual channel model. Features of characteristics. Possible MOSFET device types: n- and p-channel, enhancement and depletion mode.

**Lecture 13** -- Thursday, March 23: Summary of static large signal BJT and MOSFET models. Enhancements: base width/channel length modulation (Early effects); charge stores (diffusion and depletion stores in BJTs and MOSFETs).

**Recitation 13** -- Friday, March 24: Complete discussion of MOSFET modeling. Use of large signal model to calculate transfer characteristics of common-source inverter with resistor pull-up. *Problem Set #6 due; Problem Set #7 out (MOSFET static large signal characteristics, MOSFET types; iLab exercise - MOSFET).*

**Tutorial 7** -- Mon/Tues, April 3/4: MOSFET models, large and small signal, for n- and p-channel devices, enhancement and depletion mode.

**Lecture 14** -- Tuesday, April 4: Basic inverters as building blocks for digital logic, memory; performance criteria. Begin MOS logic; inverter options; why CMOS.

**Recitation 14** -- Wednesday, April 5: Discuss calculation of MOSFET inverter transfer characteristics; working of specific examples (saturated n-MOS pull-up, CMOS).

**Lecture 15** -- Thursday, April 6: CMOS in all its glory: Transfer characteristic calculation; including Early effect. Switching transients and minimum gate delay. Power dissipation; power density.

**Recitation 15** -- Friday, April 7: Final CMOS comments: minimum gate delay model and dynamic power dissipation model; also power dissipation at maximum data rate and power density calculations. If timer permits, transfer characteristic of source-follower stage. *Problem Set #7 due; Problem Set #8 out (transfer characteristics - hand calculation; CMOS gate delays; small signal transistor models; i-Lab exercises - Diode and BJT).*

**Tutorial 8** -- Mon/Tues, April 10/11: HSPICE for p-n diodes, BJTs, and MOSFETs. (HSPICE sessions in electronic classroom.)

**Lecture 16** -- Tuesday, April 11: Incremental models for BJT (hybrid-π) and MOSFET. npn vs. pnp; n-channel vs. p-channel; $g_o$. Early voltage; capacitances. Importance of stable bias point.
**Recitation 16** -- Wednesday, April 12: Review of incremental models. Equivalence of npn and pnp BJT lec's, and of n-channel and p-channel MOSFET lec's. Importance of bias current for static g's. Note dependence of diffusion capacitance on $g_m$. Review of all capacitances in the lec's. Typical $g_m$ and $g_s$ numbers. Applications of lec's to CMOS and nMOS transfer characteristics.


**Recitation 17** -- Friday, April 14: Example of current source design. Exercises in circuit analysis via gain, input and output resistances, etc., of common-source and common-emitter amplifiers; source- and emitter-follower amplifiers; all with resistor loads. **Problem Set #8 due; Problem Set #9 out (amplifier analysis, incl. differential amplifiers; HSPICE exercise - inverter transfer characteristic).**

**Review 2** -- Wednesday, April 19: No formal recitation sessions. Instructors will be available to answer questions and review issues for the quiz.

**Quiz 2** -- Wednesday, April 19, 7:30 to 9:30 pm, Rm 50-340 (Walker Memorial). Closed book. Covering material through 4/12/06 and Problem Set #8.

**Lecture 18** -- Thursday, April 20: Concept of mid-band frequency range. Basic single transistor amplifier building block stages: analysis and features of the common-emitter/-source, common-base/-gate, and emitter-/source-follower stages, and of stages with emitter/source degeneracy.

**Recitation 18** -- Friday, April 21: Continue/compete single-transistor amplifier stage discussion. Comparison of stages, and when and where each might be used. **Problem Set #10 out (amplifier analysis in design problem relevant contexts). Note: P.S. #9 is due Wednesday, April 26.**

**Tutorial 9** -- Mon/Tues, April 24/25: Single transistor amplifier stage examples.

**Lecture 19** -- Tuesday, April 25: Differential amplifiers: large signal analysis and transfer characteristics; incremental analysis and half-circuit analysis techniques. Example of use to simplify the analysis of a complex multi-stage amplifier circuit (i.e., the design problem circuit).

**Recitation 19** -- Wednesday, April 26: Discuss differential amplifier issues with focus on source coupled pair: review of large signal analysis; common-mode swing; full incremental analysis by decomposing inputs into difference and common mode inputs; doing half-circuit analysis, and recovering total output signals. **Problem Set #9 due. Design problem out.**

**Lecture 20** -- Thursday, April 27: Achieving maximum gain while staying in forward active region: resistor loads, non-linear loads, active loads (current mirror, Lee load, double- to single-ended output conversion). Selecting bias point for maximum gain. Examples taken from design problem circuit. *Drop Date.*

**Recitation 20** -- Friday, April 28: Overview of design problem circuit. Understanding the performance specifications: gain stage analysis; output stages; biasing issues; common- and difference-mode voltage ranges. **Problem Set #10 out (amplifier analysis in design problem relevant contexts; no due date; not graded).**

**Tutorial 10** -- Mon/Tues, May 1/2: Design problem issues.

**Lecture 21** -- Tuesday, May 2: Through the design problem from left to right. Active loads and getting maximum gain: Lee load; current mirror loads. Cascode gain stages and loads. Emitter follower output stages.
Recitation 20 -- Wednesday, May 3: Continued consideration of multi-stage differential amplifiers, design problem concerns.

Lecture 22 -- Thursday, May 4: Continued discussion of specialized stages in design problem context and other ICs, including a commercial op-amp (μA 741); use to discuss Darlington, Cascode, Push-pull, etc., as well as using a capacitor to stabilize circuit.

Recitation 22 -- Friday, May 5: General Miller capacitance phenomenon. Lack of Miller capacitance in common-gate/-base and followers. Final design problem comments.


Lecture 23 -- Tuesday, May 9: Bounding mid-band; methods of open- and of short-circuit time constants in high frequency analysis of multi-stage amplifiers. High frequency gain of common-emitter/-source stage; Miller capacitance. The value of the cascode for high frequency design.

Recitation 23 -- Wednesday, May 10: IC Fabrication technology; Berkeley CMOS fabrication video.

Lecture 24 -- Thursday, May 11: Intrinsic limits to high freq. performance of MOSFETs and BJTs: \( \omega_A, \omega_B, \omega_t \). Limits of quasi-static approx.

Recitation 24 -- Friday, May 12: High frequency analysis; method of open-circuit time constants; OCTC example. Design Problem due by 5 pm in Room 13-3058; Problem Set #11 out (ungraded set on high frequency performance; switching transients).

Tutorial 12 -- Mon/Tues, May 15/16: Discussion of design problem solution, and consideration of the high frequency performance of the circuit.


Recitation 25 -- Wednesday, May 17: Complete discussion of scaling. Driving signals off-chip; digital buffer ideas, issues, and design.

Lecture 26 -- Thursday, May 18: Overview of the IC industry, analog and digital. Review of course and suggestions for follow-on subjects.

Final -- Wednesday, May 24: Johnston Ice Rink, 1:30 to 4:30 pm. Closed book. Covering all of the material in the subject.