Lecture 18 - Single Transistor Amplifier Stages - Outline

- **Announcements**
  - Handouts - Lecture Foils
    - Notes on Single Transistor Amplifiers

- **Review - Biasing and amplifier metrics**
  - **Current mirrors in emitter and source circuits**
  - **Performance metrics:** gains (voltage, current, power); input and output resistances; power dissipation; bandwidth

- **Mid-band analysis**
  - **Biasing capacitors:** short circuits above $\omega_{LO}$
  - **Device capacitors:** open circuits below $\omega_{HI}$
  - **Midband:** $\omega_{LO} < \omega < \omega_{HI}$

- **Building-block stages**
  - **Common emitter/source**
  - **Common base/gate**
  - **Emitter/source follower** (also called common collector/drain)
  - **Series feedback** (more commonly: emitter/source degeneracy)
  - **Shunt feedback**
• Linear equivalent circuit for transistors (dynamic):

Collecting our results for the MOSFET and BJT biased in FAR

**BJT:**

\[ g_m = \frac{q}{kT} \beta_o I_{BS} e^{qV_{BE}/kT} \left[ 1 + \lambda V_{CE} \right] \approx \frac{qI_C}{kT} \]

\[ g_\pi = \frac{g_m}{\beta_o} = \frac{qI_C}{\beta_o kT} \]

\[ g_o = \beta_o I_{BS} \left[ e^{qV_{BE}/kT} + 1 \right] \lambda \approx \lambda I_C = \frac{I_C}{V_A} \]

\[ C_\pi = g_m \tau_b + \text{B-E depletion cap.} \quad \tau_b = \frac{w^2}{2D_e}, \quad C_\mu: \quad \text{B-C depletion cap.} \]

**MOSFET:**

\[ g_m = K [V_{GS} - V_T (V_{BS})] \left[ 1 + \lambda V_{DS} \right] \approx \sqrt{2KI_D} \]

\[ g_o = \frac{K}{2} [V_{GS} - V_T (V_{BS})]^2 \lambda \approx \lambda I_D = \frac{I_D}{V_A} \]

\[ g_{mb} = \eta g_m = \eta \sqrt{2KI_D} \]

\[ g_m = \eta g_m = \eta \sqrt{2KI_D} \]

with \[ \eta = -\frac{\partial V_T}{\partial V_{BS}} \bigg|_Q = \frac{1}{C_{ox}^*} \sqrt{\frac{e_s qN_A}{q \phi_p - V_{BS}}} \]

\[ C_{gs} = \frac{2}{3} W L C_{ox}^*, \quad C_{sb}, C_{gb}, C_{db} : \quad \text{depletion capacitances} \]

\[ C_{gd} = W C_{gd}^*, \text{ where } C_{gd}^* \text{ is the G-D fringing and overlap capacitance per unit gate length (parasitic)} \]
- BJTs and MOSFETs biased for linear amplifier applications
• Examples of current mirror biased BJT circuits:

- BJT Mirror: $I_C \approx (A_{Q3}/A_{Q2}) \, I_{REF}$
- MOSFET Mirror: $I_C \approx (K_{Q3}/K_{Q2}) \, I_{REF}$
• **Looking at a complicated circuit:**
  
  Lesson I - Find the biasing circuitry and represent it symbolically

Consider the following example:

11 of the 29 transistors are used for biasing the other 18 transistors.

If we get the biasing transistors out of the picture for awhile, the circuit looks simpler. *(next foil)*

Clif Fonstad, 4/20/06

Lecture 18 - Slide 5
• Looking at a complicated circuit:
  Lesson 1, cont. - Redrawing the schematic with current sources

Representing the current sources symbolically lets you focus on the action:

18 transistors are still left. In Lessons II and III we will reduce the number to 4! Stay tuned… (Lec 19)
- **Linear amplifier layouts:**

  The practical ways of putting inputs to, and taking outputs from transistors for form linear amplifiers

  There are 12 choices: three possible nodes to connect to the input, and for each one, two nodes from which to take an output, and two choices of what to do with the remaining node (ground it or connect it to something).

  Not all these choices work well, however. In fact only four do:

<table>
<thead>
<tr>
<th>Name</th>
<th>Input</th>
<th>Output</th>
<th>Grounded</th>
</tr>
</thead>
<tbody>
<tr>
<td>Common source/emitter</td>
<td>1</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>Common gate/base</td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Common drain/collector (Source/emitter follower)</td>
<td>1</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>Source/emitter degeneration</td>
<td>1</td>
<td>2</td>
<td>none</td>
</tr>
</tbody>
</table>
• Three MOSFET single-transistor amplifiers
• Single-transistor amplifiers with feedback

Parallel feedback
also termed "emitter degeneracy"

Series feedback
• Linear amplifier performance metrics:

The characteristics of linear amplifiers that we use to compare different amplifier designs, and to judge their performance and suitability for a given application are given below:

Voltage gain, \( A_v = \frac{v_{out}}{v_{in}} \)

Current gain, \( A_i = \frac{i_{out}}{i_{in}} \)

Power gain, \( A_{power} = \frac{P_{out}}{P_{in}} = \frac{v_{out}i_{out}}{v_{in}i_{in}} = A_vA_i \)

Input resistance, \( r_{in} = \frac{v_{in}}{i_{in}} \)

Output resistance, \( r_{out} = \frac{v_{test}}{i_{test}} \) with \( v_{in} = 0 \)

DC Power dissipation, \( P_{DC} = (V_+ - V_-)(\sum I_{BIAS}'s) \)
• The "mid-band" concept: frequency range of constant gain and phase

**Common emitter example:**
The linear equivalent circuit for the common emitter amplifier stage on the left is drawn below with all of the elements included:

The capacitors are of two types:
- **Biasing capacitors:** they are typically very large (in µF range) and will be effective shorts above some $\omega_{LO}$
- **Device capacitors:** they are typically very small (in pF range) and will be effective open circuits above $\omega_{HI}$
• The "mid-band" concept, cont.

At frequencies above some value ($\equiv \omega_{LO}$) the biasing capacitors look like shorts:

\[ \omega_{LO} < \omega \]

At frequencies below some value ($\equiv \omega_{HI}$) the device capacitors look like open circuits:

\[ \omega < \omega_{HI} \]
• The "mid-band" concept, cont.

If $\omega_{LO} < \omega_{HI}$, then there is a range of frequencies where all of the capacitors are either short circuits (the biasing capacitors) or open circuits (the device capacitors), and we have:

$$\omega_{LO} < \omega < \omega_{HI}$$

We call the frequency range between $\omega_{LO}$ and $\omega_{HI}$, the "mid-band" range. For frequencies in this range our model is simply:

Valid for $\omega_{LO} < \omega < \omega_{HI}$, the "mid-band" range, where all bias capacitors are shorts and all device capacitors are open.
The mid-band range of frequencies:

In this range of frequencies the gain is a constant, and the phase shift between the input and output is also constant (either 0° or 180°).

All of the parasitic capacitances are effectively open circuits

All of the biasing and coupling capacitors are effectively short circuits

* We will learn how to estimate $\omega_{HI}$ and $\omega_{LO}$ in Lecture 22.
• Common emitter/source amplifiers

![Common emitter amplifier diagram]

**Mid-band LEC for common emitter**

\( g_l \) = conductance of "LOAD" and anything connected at "\( v_{out} \)"

<table>
<thead>
<tr>
<th>Component</th>
<th>BJT</th>
<th>MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>( A_v )</td>
<td>(-\frac{g_m}{g_o + g_l})</td>
<td>(-\frac{g_m}{g_o + g_l})</td>
</tr>
<tr>
<td>( A_i )</td>
<td>(-\beta \frac{g_l}{g_o + g_l})</td>
<td>(\infty)</td>
</tr>
<tr>
<td>( R_{in} )</td>
<td>(r_\pi)</td>
<td>(\infty)</td>
</tr>
<tr>
<td>( R_{out} )</td>
<td>(\frac{1}{g_o} = r_o)</td>
<td>(\frac{1}{g_o} = r_o)</td>
</tr>
</tbody>
</table>

A good workhorse gain stage
• Emitter/source followers

\[ V_+ \]

\[ V_- \]

\[ \text{Emitter Follower} \]

\[ \text{CO} \]

\[ \text{I}_{\text{BIAS}} \]

\[ V_{\text{in}} \]

\[ V_{\text{out}} \]

\[ g_l = \text{conductance of "} I_{\text{BIAS}} \text{" and anything connected at } V_{\text{out}}\]

- A great output buffer stage with small \( R_{\text{out}} \), big \( R_{\text{in}} \)

\[
A_v: \quad \frac{1}{1 + (g_o + g_l)/(g_m + g_\pi)} \approx 1 \\
A_i: \quad \beta \frac{g_l}{(g_o + g_l)} \approx \infty \\
R_{\text{in}}: \quad \frac{1}{g_\pi} + \frac{(\beta + 1)(g_o + g_l)}{g_m} = r_\pi + (\beta + 1) \frac{r_o \| r_l}{g_m} \approx \infty \\
R_{\text{out}}: \quad \frac{g_o + g_l + (g_m + g_\pi)}{(1 + g_\pi r_t)^{-1}} \approx \frac{(r_t + r_\pi)/(\beta + 1)}{g_m} \approx 1/g_m
\]
• Common base/gate amplifiers

Mid-band LEC for common gate
$g_l =$ conductance of "LOAD" and anything connected at "$v_{out}$"
The conductance of $I_{BIAS}$ can be neglected.

**BJT**

$A_v: \frac{(g_m+g_o)}{(g_l+g_o)} \approx g_m \left(\frac{r_l}{r_o}\right)$

$A_i: \frac{(g_m+g_o)}{(g_m+g_o+g_{\pi}+g_{\pi}g_o/g_l)} \approx 1$

$R_{in}: \left[\frac{g_m+g_{\pi}+g_o(g_l-g_m)}{(g_l+g_o)}\right]^{-1} \approx \frac{1}{(g_m+g_{\pi})} = \frac{r_{\pi}}{(\beta+1)}$

$R_{out}: r_o \left[1 + \frac{(g_m+g_o)}{(g_{\pi}+g_t)}\right] \approx (\beta+1)r_o$

**MOSFET**

$A_v: \frac{(g_m+g_{mb}+g_o)}{(g_l+g_o)} \approx (g_m+g_{mb}) \left(\frac{r_l}{r_o}\right)$

$A_i: \frac{(g_m+g_{mb}+g_o)}{(g_m+g_o+g_{\pi}+g_{\pi}g_o/g_l)} \approx 1$

$R_{in}: \left[\frac{g_m+g_{mb}+g_o(g_l-g_m)}{(g_l+g_o)}\right]^{-1} \approx \frac{1}{(g_m+g_{mb})}$

$R_{out}: r_o \left[1 + \frac{(g_m+g_{mb}+g_o)}{g_t}\right] \approx (\beta+1)r_o$

• A very low $R_{in}$, large $R_{out}$ stage often used to complement other stages
• Series Feedback: emitter/source degeneracy

Emitter degeneracy

Mid-band LEC for degenerate emitter
\[ g_i = \text{conductance of "LOAD" and anything connected at "v_{out}"} \]

\[
\begin{align*}
A_v : & \approx -r_l/R_F \\
A_i : & \approx \beta \\
R_{in} : & \approx r_\pi + (\beta+1)R_F \\
R_{out} : & \approx 1/g_o
\end{align*}
\]

Useful in discrete device circuit design; we use to understand common-mode gain suppression in differential amplifiers
• **Feedback:** shunt feedback element

![Circuit Diagram]

**Mid-band LEC for a shunted common-emitter**

\[ g_i = \text{conduction of "LOAD" and anything connected at "} v_{out}\text{"} \]

- **BJT**
  - \( A_v : \frac{-g_m - G_F}{g_o + G_F} \)
  - \( A_i : -g_m R_F \)
  - \( R_{in} : \frac{1}{g_{\pi} + G_F(1-A_v)} \)
  - \( R_{out} : (r_o || R_F) \)

- **MOSFET**
  - \( A_v : \frac{-g_m - G_F}{g_o + G_F} \)
  - \( A_i : -g_m R_F \)
  - \( R_{in} : \frac{R_F}{1-A_v} \)
  - \( R_{out} : (r_o || R_F) \)

Used to stabilize high gain circuits and in transimpedance amplifiers; the same topology leads to the Miller effect (Lec. 24).
## Summary of the single transistor stages (bipolar)

<table>
<thead>
<tr>
<th>BIPOLAR</th>
<th>Voltage gain, $A_v$</th>
<th>Current gain, $A_i$</th>
<th>Input resistance, $R_i$</th>
<th>Output resistance, $R_o$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Common emitter</td>
<td>$- \frac{g_m}{g_o + g_l}$ ($= -g_m r'_l$)</td>
<td>$- \frac{\beta g_l}{g_o + g_l}$</td>
<td>$r_\pi$</td>
<td>$r_o \left( = \frac{1}{g_o} \right)$</td>
</tr>
<tr>
<td>Common base</td>
<td>$\frac{g_m}{g_o + g_l}$ ($= g_m r'_l$)</td>
<td>$\approx 1$</td>
<td>$\approx \frac{r_\pi}{\beta + 1}$</td>
<td>$\approx [\beta + 1]r_o$</td>
</tr>
<tr>
<td>Emitter follower</td>
<td>$\frac{g_m + g_\pi}{g_m + g_\pi + g_o + g_l}$</td>
<td>$\approx 1$</td>
<td>$\approx r_\pi + [\beta + 1]r'_i$</td>
<td>$\approx r_o$</td>
</tr>
<tr>
<td>Emitter degeneracy</td>
<td>$\approx -\frac{r'_i}{R_F}$</td>
<td>$\approx \beta$</td>
<td>$\approx r_\pi + [\beta + 1]R_F$</td>
<td>$\approx r_o$</td>
</tr>
<tr>
<td>Shunt feedback</td>
<td>$- \frac{g_m - G_F}{g_o + G_F}$</td>
<td>$- \frac{g_l}{G_F}$</td>
<td>$1 \over g_\pi + G_F(1 - A_v)$</td>
<td>$r_o \parallel R_F \left( = \frac{1}{g_o + G_F} \right)$</td>
</tr>
</tbody>
</table>
• **Summary of the single transistor stages (MOSFET)**

<table>
<thead>
<tr>
<th>MOSFET</th>
<th>Voltage gain, $A_v$</th>
<th>Current gain, $A_i$</th>
<th>Input resistance, $R_i$</th>
<th>Output resistance, $R_o$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Common source</td>
<td>$-\frac{g_m}{g_o + g_l} \left( = -g_m r_i^l \right)$</td>
<td>$\infty$</td>
<td>$\infty$</td>
<td>$\frac{1}{g_o}$</td>
</tr>
<tr>
<td>Common gate</td>
<td>$\approx g_m + g_{mb} r_i^l$</td>
<td>$\approx 1$</td>
<td>$\approx \frac{1}{g_m + g_{mb}}$</td>
<td>$\approx r_o \left{ 1 + \frac{g_m + g_{mb} + g_o}{g_t} \right}$</td>
</tr>
<tr>
<td>Source follower</td>
<td>$\frac{g_m + g_\pi}{g_m + g_o + g_l} \approx 1$</td>
<td>$\infty$</td>
<td>$\infty$</td>
<td>$\approx \frac{1}{g_m}$</td>
</tr>
<tr>
<td>Source degeneracy (series feedback)</td>
<td>$\approx -\frac{r_i^l}{R_F}$</td>
<td>$\infty$</td>
<td>$\infty$</td>
<td>$\approx r_o$</td>
</tr>
<tr>
<td>Shunt feedback</td>
<td>$-\frac{g_m - G_F}{g_o + G_F} \approx -g_m R_F$</td>
<td>$-\frac{g_l}{G_F}$</td>
<td>$\frac{1}{G_F \left[ 1 - A_v \right]}$</td>
<td>$r_o \parallel R_F \left( = \frac{1}{\left[ g_o + G_F \right]} \right)$</td>
</tr>
</tbody>
</table>
• Mid-band analysis
  
  **Biasing capacitors:** typically in \( \mu F \) range
  should/can be avoided completely in modern IC design \((\omega_{LO} = 0)\)

  **Device capacitors:** typically in pF range; goal is to make as small as possible

  **Midband:** no capacitors in incremental analysis; gain and phase constant
  want as wide as possible
  
  \( \text{we won't find } \omega_{LO} \text{ and } \omega_{HI} \text{ until Lec. 22} \)

• Building-block stages
  
  **Common emitter/source:** good voltage and current gain
  large \( R_{in} \) and \( R_{out} \)
  good gain stage

  **Common base/gate:** very small \( R_{in} \); very large \( R_{out} \)
  unity current gain; good voltage gain
  will find paired with other stages to form "cascode"

  **Emitter/source follower:** very small \( R_{out} \); very large \( R_{in} \)
  unity voltage gain; good current gain
  an excellent output stage or buffer

  **Series feedback:** moderate voltage gain dependant on ratio of resistors

  **Shunt feedback:** used in transimpedance amplifiers