Announcements
Handouts - Lecture Foils
Design Problem - out tomorrow in recitation

Review - Single-transistor building block stages
Common emitter/source: general purpose gain stage, workhorse
Common base/gate: small $R_{in}$, large $R_{out}$, unity $A_i$, same $A_v$ as CE/S
Emitter/source follower: large $R_{in}$, small $R_{out}$, unity $A_v$, same $A_i$ as CE/S
Series and Shunt feedback: we'll see in special situations

Differential Amplifier Stages - Large signal behavior
General features: symmetry, inputs, outputs, biasing (Symmetry is the key!)
Large signal transfer characteristic

Difference- and common-mode signals
Decomposing and reconstructing general signals

Half-circuit incremental analysis techniques
Linear equivalent half-circuits
Difference- and common-mode analysis
Example: analysis of emitter-coupled pair
• The "mid-band" concept: frequency range of constant gain and phase

**LEC for common emitter stage valid at all frequencies**

- **Biasing capacitors:** typically in µF range
  - (C_O, C_E, etc.)
  - effectively shorts above \( \omega_{LO} \)
- **Device capacitors:** typically in pF range
  - (C_π, C_µ, etc.)
  - effectively open ckt's until \( \omega_{HI} \)
- **Mid-band frequencies:** defined as \( \omega_{LO} < \omega < \omega_{HI} \)

**Common emitter LEC for in mid-band range**

(Note: \( g_I = g_{LOAD} + g_{next} \) )
• Summary of the single transistor stages (bipolar)

<table>
<thead>
<tr>
<th>BIPOLAR</th>
<th>Voltage gain, $A_v$</th>
<th>Current gain, $A_i$</th>
<th>Input resistance, $R_i$</th>
<th>Output resistance, $R_o$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Common emitter</td>
<td>$-\frac{g_m}{g_o + g_l}$ ($=-g_m r_i'$)</td>
<td>$-\frac{\beta g_l}{g_o + g_l}$</td>
<td>$r_\pi$</td>
<td>$r_o \left( = \frac{1}{g_o} \right)$</td>
</tr>
<tr>
<td>Common base</td>
<td>$\frac{g_m}{g_o + g_l}$ ($=g_m r_l'$)</td>
<td>$\approx 1$</td>
<td>$\approx \frac{r_\pi}{[\beta + 1]}$</td>
<td>$r_o \left[ 1 + \frac{(g_m + g_o)}{(g_\pi + g_l)} \right] \approx [\beta + 1]r_o$</td>
</tr>
<tr>
<td>Emitter follower</td>
<td>$\frac{[g_m + g_\pi]}{[g_m + g_\pi + g_o + g_l]} \approx 1$</td>
<td>$\frac{\beta g_l}{g_o + g_l} \approx \beta$</td>
<td>$r_\pi + [\beta + 1]r_l'$</td>
<td>$r_i + r_\pi \left( = \frac{[\beta + 1]}{[\beta + 1]} \right)$</td>
</tr>
<tr>
<td>Emitter degeneracy</td>
<td>$\approx -\frac{r_i}{R_F}$</td>
<td>$\approx \beta$</td>
<td>$\approx r_\pi + [\beta + 1]R_F$</td>
<td>$\approx r_o$</td>
</tr>
<tr>
<td>Shunt feedback</td>
<td>$-\frac{[g_m - G_F]}{[g_o + G_F]} \approx -g_m R_F$</td>
<td>$-\frac{g_l}{G_F}$</td>
<td>$\frac{1}{g_\pi + G_F[1 - A_v]}$</td>
<td>$r_o \parallel R_F \left( = \frac{1}{g_o + G_F} \right)$</td>
</tr>
</tbody>
</table>
• **Summary of the single transistor stages (MOSFET)**

<table>
<thead>
<tr>
<th>MOSFET</th>
<th>Voltage gain, $A_v$</th>
<th>Current gain, $A_i$</th>
<th>Input resistance, $R_i$</th>
<th>Output resistance, $R_o$</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Common source</strong></td>
<td>$-\frac{g_m}{g_o + g_l} = -g_m r_i'$</td>
<td>$\infty$</td>
<td>$\infty$</td>
<td>$r_o \left( = \frac{1}{g_o} \right)$</td>
</tr>
<tr>
<td><strong>Common gate</strong></td>
<td>$\approx [g_m + g_{mb}] r_i'$</td>
<td>$\approx 1$</td>
<td>$\approx \frac{1}{g_m + g_{mb}}$</td>
<td>$\approx r_o \left{ 1 + \frac{g_m + g_{mb} + g_o}{g_t} \right}$</td>
</tr>
<tr>
<td><strong>Source follower</strong></td>
<td>$\frac{g_m + g_{\pi}}{g_m + g_o + g_l} \approx 1$</td>
<td>$\infty$</td>
<td>$\infty$</td>
<td>$\frac{1}{g_m + g_o + g_l} \approx \frac{1}{g_m}$</td>
</tr>
<tr>
<td><strong>Source degeneracy</strong></td>
<td>$\approx -\frac{r_i}{R_F}$</td>
<td>$\infty$</td>
<td>$\infty$</td>
<td>$\approx r_o$</td>
</tr>
<tr>
<td><strong>(series feedback)</strong></td>
<td>$\approx -\frac{g_m - G_F}{g_o + G_F} \approx -g_m R_F - \frac{g_l}{G_F} \frac{1}{G_F[1 - A_v]}$</td>
<td>$1 \frac{G_F}{G_F[1 - A_v]}$</td>
<td>$R_o \parallel R_F \left( = \frac{1}{g_o + G_F} \right)$</td>
<td></td>
</tr>
</tbody>
</table>
Differential Amplifiers: emitter- and source-coupled pairs

Emitter-coupled pair

Source-coupled pair

Why do we care? -
They amplify only difference-mode signals
They are easy to interconnect and cascade
They help us eliminate coupling capacitors
They are optimally suited to integration
Differential Amplifiers: large signal analysis of emitter coupled pairs

Emitter-coupled pair
Below: Schematic with resistor loads
Right: Large signal equivalent circuit in FAR

Analysis:

3 KVL loops: \( v_{i1} - v_{BE1} + v_{BE2} - v_{i2} = 0 \), \( v_{O1} = V_{CC} - R_C \alpha_F i_{F1} \), \( v_{O2} = V_{CC} - R_C \alpha_F i_{F2} \)

KCL at one node: \( i_{F1} + i_{F2} = I_{BIAS} \)

Ideal diode relationships: \( i_{F1} \approx I_{ES} \exp \left( \frac{q v_{BE1}}{kT} \right) \), \( i_{F2} \approx I_{ES} \exp \left( \frac{q v_{BE2}}{kT} \right) \)

(see text for details of analysis)

Clif Fonstad, 4/25/06
**Diff. Amps:** large signal analysis of emitter coupled pairs, cont.

**Results:** The outputs only depend on the difference between the two inputs, \((v_{11} - v_{12}) :\)

\[
v_{O1} = V_{CC} - \frac{\alpha_F R_C I_{BIAS}}{1 + e^{-q(v_{11} - v_{12})/kT}}
\]

\[
v_{O2} = V_{CC} - \frac{\alpha_F R_C I_{BIAS}}{1 + e^{q(v_{11} - v_{12})/kT}}
\]

\[
v_O = -\alpha_F R_C I_{BIAS} \tanh \left( \frac{q(v_{11} - v_{12})}{2kT} \right)
\]

Symmetrical

Slope around origin = \(-g_m R_C\)

Only the difference in the inputs matters!!
Differential Amplifiers: large signal analysis of source coupled pairs

**Source-coupled pair**

Below: Schematic with resistor loads
Right: Large signal equiv. circuit in saturation

**Differential Amplifiers:**

**Source-coupled pair**

**Analysis:**

3 KVL loops: \(v_{I1} - v_{GS1} + v_{GS2} - v_{I2} = 0\), \(v_{O1} = V_{DD} - R_D i_{D1}\), \(v_{O2} = V_{DD} - R_D i_{D2}\)

KCL at one node: \(i_{D1} + i_{D2} = I_{BIAS}\)

MOSFET relationships: \(i_{D1} = K(v_{GS1} - V_T)^2 / 2\); \(i_{D2} = K(v_{GS2} - V_T)^2 / 2\)

Clif Fonstad, 4/25/06

(see text for details of analysis)
**Diff. Amps:** large signal analysis of source coupled pairs, cont.

**Results:** The outputs again only depend on the difference between the two inputs, \((v_{I1} - v_{I2})\):

\[
\begin{align*}
  v_{O1} &= V_{DD} - \frac{R_D}{2} \left\{ K \left[ v_{IN1} - v_{IN2} \right]^2 + I_{BIAS} \right. \\
  & \quad + \frac{K}{2} \left[ v_{IN1} - v_{IN2} \right] \sqrt{\frac{4I_{BIAS}}{K}} - \left[ v_{IN1} - v_{IN2} \right]^2 \\
  v_{O2} &= V_{DD} - \frac{R_D}{2} \left\{ K \left[ v_{IN1} - v_{IN2} \right]^2 + I_{BIAS} \right. \\
  & \quad - \frac{K}{2} \left[ v_{IN1} - v_{IN2} \right] \sqrt{\frac{4I_{BIAS}}{K}} - \left[ v_{IN1} - v_{IN2} \right]^2 \\
  v_O &= -\frac{R_D K}{2} \left[ v_{IN1} - v_{IN2} \right] \sqrt{\frac{4I_{BIAS}}{K}} - \left[ v_{IN1} - v_{IN2} \right]^2
\end{align*}
\]

Slope around origin = \(-g_m R_D\)

Only the difference in the inputs matters!!
Differential Amplifier Analysis -
difference- and common-mode signals

Any pair of signals can be decomposed into a portion that is the identical in both, and a portion that is equal, but opposite in both. For example, if we have two voltages, $v_1$ and $v_2$, we can define a common-mode signal, $v_C$, and a difference-mode signal, $v_D$, as:

$$v_C = \frac{(v_1 + v_2)}{2} \quad v_D = v_1 - v_2$$

In terms of these two voltages, we can write $v_1$ and $v_2$ as:

$$v_1 = v_C + \frac{v_D}{2} \quad v_2 = v_C - \frac{v_D}{2}$$

In incremental analysis of linear amplifiers we will decompose our inputs into difference- and common-mode inputs:

$$v_{ic} = \frac{(v_{in1} + v_{in2})}{2} \quad \text{and} \quad v_{id} = v_{in1} - v_{in2}.$$  

We will apply $v_{id}$ to the circuit and get $v_{od} (= A_{vd}v_{id})$, and then apply $v_{ic}$ to the circuit to get $v_{oc} (= A_{vc}v_{ic})$. Then we will reconstruct our outputs:

$$v_{out1} = v_{oc} + \frac{v_{od}}{2} = A_{vc}v_{ic} + A_{vd}\frac{v_{id}}{2}$$

$$v_{out2} = v_{oc} - \frac{v_{od}}{2} = A_{vc}v_{ic} - A_{vd}\frac{v_{id}}{2}$$
Differential Amplifier Analysis - incremental analysis exploiting symmetry and superposition

Linear equivalent circuit (symmetrical)

-a LEHC: one half of sym. LEC

-a LEHC: one half of sym. LEC
Differential Amplifier Analysis - incremental analysis exploiting symmetry and superposition

\[ V_{od} = A_{vd} V_{id} \]

\[ V_{oc} = A_{vc} V_{ic} \]

No voltage on common links, so incrementally they are grounded.

No current in common links, so incrementally they are open.
• **Looking at a complicated circuit:**

  *Lesson II - Identify the individual stages and their active transistors and load elements.*

Continuing with our earlier example, consider the following:

![Circuit Diagram]

**Note:** We can almost make sense of all of the stages, but we will need to study active loads, the cascode, and output stages to completely understand them.
• Looking at a complicated circuit:

Lesson III - Use half-circuit techniques to convert the differential stages to familiar single transistor stages.

Continuing with the same example:

There are two symmetrical differential gain stages, followed by two complimentary output stages* (next foil)
• Looking at a complicated circuit:
  Lesson III, cont. - Draw the difference and common mode half circuits.

Difference mode half circuit:

Common mode half circuit:

Voila!! We have reduced the transistor count from 29 to 4, and we see that complex our amplifier is a just cascade of 4 single-transistor stages.
6.012 - Microelectronic Devices and Circuits
Lecture 19 - **Differential Amplifier Stages** - Summary

- **Differential Amplifier Stages - Large signal behavior**
  
  **General features:**
  - two transistors (an emitter-coupled, or source-coupled, pair)
  - highly symmetrical
  - two inputs, two outputs (however, one input can be zero)
  - biased by single current source

  **Large signal transfer characteristics:** only depends on \( v_{IN1} - v_{IN2} \)

- **Difference- and common-mode signals**
  
  **Difference-mode:** \( v_{ID} = v_{IN1} - v_{IN2} \)
  
  **Common-mode:** \( v_{IC} = (v_{IN1} + v_{IN2})/2 \)
  
  **Reconstruction:** \( v_{IN1} = v_{ID} + v_{IC}/2, v_{IN2} = v_{ID} - v_{IC}/2 \)

- **Half-circuit incremental analysis techniques**
  
  **Exploiting symmetry and superposition**
  
  **Difference-mode lin. equiv. half-circuit:** links are grounded
  
  **Common-mode lin. equiv. half circuit:** links are cut, open circuited

  **Approach:**
  1. identify common- and difference-mode half circuits
  2. calculate common- and difference-mode signals
  3. analyze difference-mode half-circuit (each half-circuit is one of our known building-blocks)
  4. analyze common-mode half-circuit
  5. reconstruct signals