6.012 Electronic Devices and Circuits

Exam No. 2

Wednesday, November 8, 1995
4-270 (a-l) and 4-370 (m-z)
7 to 9 pm

Notes:

1. Unless otherwise indicated, assume room temperature and that kT/q is 0.025 V. You may also approximate [(kT/q) ln 10] as 0.06 V.

2. Open book; 6.012 text and any other notes permitted.

3. All of your answers and any relevant work must appear on these pages. Any additional paper you hand in will not be graded.

4. Make reasonable approximations and assumptions. State and justify any such assumptions and approximations you do make.

5. Be careful to include the correct units with your answers when appropriate.

6. Be certain that you have all nine (9) pages of this exam booklet and make certain that you write your name at the top of this page in the space provided.
Problem 1 (35 points)

For many high performance MOSFET circuits it is desirable to have both n-channel and p-channel devices on the same silicon integrated circuit chip. One way to accomplish this is illustrated below.

\[ p^+, n^+: 10^{18} \text{ cm}^{-3} \quad p: 10^{16} \text{ cm}^{-3} \quad n: 10^{15} \text{ cm}^{-3} \]

The two MOSFETs shown have identical dimensions. This problem concerns, first, four bipolar junction transistors which are inadvertently formed in this process, and later, the two MOSFETs themselves. These devices and the terminals which each incorporate are listed below:

- **Bipolar transistors:**
  - \( Q_1 [S_p (= E), B_p (= B), D_p (= C)] \)
  - \( Q_2 [S_p (= E), B_p (= B), B_n (= C)] \)
  - \( Q_3 [S_n (= E), B_n (= B), D_n (= C)] \)
  - \( Q_4 [D_n (= E), B_n (= B), B_p (= C)] \)

- **MOS field-effect transistors:**
  - \( M_1 [S_p, G_p, D_p, B_p] \)
  - \( M_2 [S_n, G_n, D_n, B_n] \)

a) Which one of the bipolar transistors would you expect to have the least base width modulation, i.e. the largest Early voltage, and why?

Transistor ________ because:

b) Look at the pnp bipolar transistor \( Q_1 \)

i) Would you expect the forward current gain, \( \beta_F \), of this device to be large or small, and why?

Large ( ) Small ( ) because:

ii) How do the forward and reverse alphas, \( \alpha_F \) and \( \alpha_R \), of this transistor compare?

\( \alpha_F \) larger ( ) \( \alpha_R \) larger ( ) Both the same ( ) because:

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Problem 1 continued

iii) How do the emitter and collector saturation currents, $I_{ES}$ and $I_{CS}$ of this transistor compare?
- $I_{ES}$ larger ( )
- $I_{CS}$ larger ( )
- Both the same ( ) because:

iv) Is this transistor structure conducive to achieving small base width modulation, i.e. the Early effect, or not, and why?
- Yes ( )
- No ( )
- because:

c) This part concerns the hybrid-π models for the bipolar transistors when each is biased with a collector current, $I_C$, of 1 mA, and with $|V_{CB}| = 1$ V. (Assume that each is biased individually; it may not be possible to bias them all simultaneously.)

i) Which device, if any, has the largest value of $g_{mV}$ and why?
- $Q_1$ ( )
- $Q_2$ ( )
- $Q_3$ ( )
- $Q_4$ ( )
- All same ( )
- because:

ii) Which device, if any, has the smallest value of $C_{µV}$ and why?
- $Q_1$ ( )
- $Q_2$ ( )
- $Q_3$ ( )
- $Q_4$ ( )
- All same ( )
- because:

d) When using the MOSFETs in this structure it is important that none of the inadvertent BJTs are active. State a biasing rule of thumb that can be used to insure that none of the BJTs in this structure are biased in their forward active regions.

e) Now look at the two MOSFETs, the p-channel MOSFET, $M_1$, on the right, and the n-channel MOSFET, $M_2$, on the left. Consider the linear equivalent circuit models for these transistors when each is biased in saturation with $|I_D| = 1.0$ mA.

i) Which of these two transistors, if any, has the largest transconductance, $g_{mV}$, and why?
- $M_1$ ( )
- $M_2$ ( )
- Both same ( )
- because:

ii) Which of these two devices, if any, has the largest drain-to-substrate capacitance, $C_{db}$, and why?
- $M_1$ ( )
- $M_2$ ( )
- Both same ( )
- because:

Problem 1 continues on the next page
Problem 1 continued

iii) Which of these two devices, if any, has the largest gate-to-source capacitance, $C_{gs}$, and why?

M₁ ( ) M₂ ( ) Both same ( ) because:

f) Now focus on the p-channel MOSFET, M₁. You are given the following plot of the capacitance between the gate and the substrate (with the drain and source shorted to the substrate) as a function of voltage:

![Capacitance graph]

i) What is the threshold voltage of this device?

$V_T = \underline{\text{_____}}$

ii) What is the flat-band voltage of this device?

$V_{FB} = \underline{\text{_______}}$

iii) Is this device enhancement or depletion mode, and why?

Enhancement mode ( ) Depletion mode ( ) because:

End of Problem 1
Problem 2 (30 points)

a) Consider the symmetrical, abrupt silicon p-n junction diode illustrated below. The doping levels are both $10^{16}$ cm$^{-3}$ (i.e. $N_{Ap} = N_{Dn} = 10^{16}$ cm$^{-3}$). This device is a short base diode (i.e. $L_e >> w_p$, and $L_h >> w_n$), and $\mu_e = 2.5 \mu_h = 1,500$ cm$^2$/V-s.

This device is illuminated with light which generates $M$ hole-electron pairs per cubic centimeter per second uniformly across the plane at $x = x_l$. When $x_l$ is midway between $x_n$ and $w_n$ (i.e. when $x_l = x_n + (w_n - x_n)/2 = (w_n + x_n)/2$), the diode current, $i_D$, is $-1.0 \mu$A, and the peak excess minority carrier population, $p'(x_l)$ is $10^{15}$ cm$^{-3}$.

What is the diode current, $i_D$, when $x_l$ has each of the following values, and what are the peak excess minority carrier populations, $n'(x_l)$ or $p'(x_l)$, in each case?

i) $x_l = -(w_p + x_p)/2$ (i.e. midway between $-w_p$ and $-x_p$)

     $i_D =$ ____________

     $p'(x_l)$ or $n'(x_l) =$ ____________

ii) $x_l = x_n + (w_n - x_n)/4$ (i.e. a quarter of the way from $x_n$ to $w_n$)

     $i_D =$ ____________

     $p'(x_l)$ or $n'(x_l) =$ ____________

iii) $x_l = w_n$ (i.e. at the ohmic contact)

     $i_D =$ ____________

     $p'(x_l)$ or $n'(x_l) =$ ____________

iv) $x_l = 0$ (i.e. in the depletion region)

     $i_D =$ ____________

     $p'(x_l)$ or $n'(x_l) =$ ____________

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Problem 2 continued

b) Now consider the same p-n diode structure as in Part (a), except that now instead of being illuminated, this diode has an MOS capacitor fabricated on its side as pictured below.

When the small signal capacitance of the junction is measured as a function of the bias voltage on the MOS capacitor, $V_{GA}$, and with a bias on the diode, $V_{AB}$, of zero (0) volts, it is found that the capacitance is essentially constant until $V_{GA}$ is sufficiently positive or negative that the surface under the MOS capacitor gate on the n- or p-side of the junction becomes inverted. Then the capacitance increases; this behavior is shown in the sketch below.

i) Using the information in the sketch above, determine the threshold voltages of the MOS structures formed over the p-side and n-side of the diode, respectively.

\[
V_T(p-side) = \\
V_T(n-side) = 
\]

ii) Using your understanding of inversion layers, explain (in 25 words or less) why the zero-bias small-signal capacitance measured at the diode terminals increases after the surface has become inverted.

iii) Explain qualitatively how and why you would expect the reverse bias diode current to change as $V_{GA}$ is varied from -3 V to +3V. Assume $V_{AB} = -100$ mV. Provide a sketch if it is helpful.

End of Problem 2
Problem 3 (35 points)

Consider the two transistors, one an npn bipolar junction transistor (BJT) and the other an n-channel metal-oxide-semiconductor field effect transistor (MOSFET). We have the following information about each device:

BJT, Q_B: $\beta = 100$, $V_{BE,ON} = 0.6$ V, $V_{CE,SAT} = 0.2$ V, and $|V_A| = 50$ V.

MOSFET, Q_M: $K = 0.2$ mA/V$^2$, $V_T = 1.0$ V, and $|V_A| = 20$ V.

These devices are both used in a circuit in which they are biased so that they are in their high gain region, where by "high gain region" we mean that the BJT is in its forward active region, and the MOSFET is in saturation, and the quiescent collector and drain currents are 1 mA (i.e. $I_C = 1$ mA and $I_D = 1$ mA). For the MOSFET, $V_{BS} = 0$.

(a) For the bias level indicated above what is $V_{BE}$ on the BJT and what is $V_{GS}$ on the MOSFET?

$$V_{BE} = \text{_______________}$$

$$V_{GS} = \text{_______________}$$

(b) What is the range of possible values for the following voltages if each device is to remain in its high gain region, as defined above? Note: Not all blanks need be filled.

(i) BJT base to collector voltage, $V_{BC}$

$$\text{___________} < V_{BC} < \text{___________}$$

(ii) BJT collector to emitter voltage, $V_{CE}$

$$\text{___________} < V_{CE} < \text{___________}$$

(iii) MOSFET gate to drain voltage, $V_{GD}$

$$\text{___________} < V_{GD} < \text{___________}$$

(iv) MOSFET drain to source voltage, $V_{DS}$

$$\text{___________} < V_{DS} < \text{___________}$$
Problem 3 continued

(c) A generic linear equivalent circuit for any three terminal device is shown below:

Give parameters for this model relevant to each of the two transistors in this problem at the bias point stated above (i.e. $I_C = I_D = 1$ mA, bias in high gain region).

For BJT: $g_i = \quad \quad g_r =$

$g_m = \quad \quad g_o =$

For MOSFET: $g_i = \quad \quad g_r =$

$g_m = \quad \quad g_o =$

(d) Select $R_E$ in the circuit illustrated below so that the bipolar transistor, $Q_B$, is biased with $I_C = 1$ mA.

$R_E =$

Problem 3 continues on the next page
Problem 3 continued

(e) (i) In the space provide below, draw a mid-band frequency range small signal linear equivalent circuit for the circuit on the preceding page.

(ii) Calculate the mid-band small signal voltage gain, $A_v$, of this circuit.

\[ A_v = \text{__________} \]

(f) (i) What is the total quiescent (DC) current supplied by the 6V supply in this circuit?

Current from supply: \[\text{__________}\]

(ii) What is the total quiescent (DC) power dissipated in this circuit?

Power dissipated in circuit: \[\text{__________}\]

End of Problem 3

End of Exam