Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.071 – Introduction to Electronics, Signals and Measurement
Spring 2005
Final

• Please write your name on each page of the exam in the space provided
• Please verify that there are 19 pages in your exam.
• To the extent possible, do your work for each question within the boundaries of the question or on the back side or the page preceding the question. Extra pages are also provided for computation.
• Note that the total number of points is 100.
• Closed book. No notes. No Calculators

Solutions
Diodes:

- **Ideal diode model**
  - Anode
  - Cathode
  - \( I_d + V_d = -\) 

- **0.7 Volt offset model**
  - \( V_g = 0.7 \text{ Volts} \)
  - \( I_d + V_d = -\)

- **Full diode model**
  - \( I_d = I_s \left[ \exp \left( \frac{V_d}{V_r} \right) - 1 \right] \)

- **Zener Diode**
  - \( V_Z \)
  - Ideal model
  - \( I_d \rightarrow V_Z \rightarrow I_d \)

Reactive Elements:

- **Capacitor**
  - \( I_c = C \frac{dV_c}{dt} \)
  - \( Z_C = \frac{j}{\omega C} \)

- **Inductor**
  - \( V_L = L \frac{dI_L}{dt} \)
  - \( Z_L = j\omega L \)

Decibel definition: \( dB = 20 \log \frac{A_o}{A_i} \)

6.071 Final  Page: 2
Op-Amps

Ideal Op-amp model (negative feedback)

\[ I_+ = I_- = 0 \]
\[ V_+ = V_- \]

Ideal 3 state op-amp model (open loop and positive feedback)

\[ I_+ = I_- = 0 \]
\[ V_{C+} = \begin{cases} A(V_+ - V_-), & \text{for } A(V_+ - V_-) > V_{C+}; \text{ non-linear} \\ V_{C-}, & \text{for } A(V_+ - V_-) < V_{C-}; \text{ linear} \end{cases} \]
\[ V_{O} = \begin{cases} A(V_+ - V_-), & \text{for } A(V_+ - V_-) < V_{C+}; \text{ non-linear} \end{cases} \]

BJTs

\[ I_c = I_c + I_b \]

For operation in the active region
\[ I_c = \beta I_b \]
\[ V_{be} = 0.7 \text{ V} \]

FETs

In the ohmic region
\[ I_s = I_{os} \left[ -2 \left( 1 - \frac{V_{gs}}{V_{gs,off}} \right) \left( \frac{V_{gs}}{V_{gs,off}} \right)^2 \right] \]

In the saturation region
\[ I_s = I_{os} \left( 1 - \frac{V_{gs}}{V_{gs,off}} \right)^2 \]

6.071 Final
### Useful Information

**Boolean Identities**

<table>
<thead>
<tr>
<th>Boolean Identity</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>(A + 0 = A)</td>
<td>(A \cdot 1 = A)</td>
</tr>
<tr>
<td>(A + B = B + A)</td>
<td>(A'B = BA)</td>
</tr>
<tr>
<td>(A + (B + C) = (A + B) + C)</td>
<td>(A(BC) = (AB)C)</td>
</tr>
<tr>
<td>(A + BC = (A + B)(A + C))</td>
<td>(A(B + C) = AB + AC)</td>
</tr>
<tr>
<td>(A + A = A)</td>
<td>(A \cdot \bar{A} = 0)</td>
</tr>
<tr>
<td>(A + !A = 1)</td>
<td>(A \cdot 0 = 0)</td>
</tr>
<tr>
<td>(A \cdot AB = A)</td>
<td>(A(A + B) = A)</td>
</tr>
<tr>
<td>(A + A \cdot B = A + B)</td>
<td>((A + B)(A + C) = A + B\ C)</td>
</tr>
<tr>
<td>(\bar{A}B = A + B)</td>
<td>(A + B = A \cdot B)</td>
</tr>
</tbody>
</table>

### RS Flip-Flop

- **Truth Table**
  - \(R\) = 0, \(S\) = 0: \(Q_{n+1} = Q_n\)
  - \(R\) = 0, \(S\) = 1: \(Q_{n+1} = 1\)
  - \(R\) = 1, \(S\) = 0: \(Q_{n+1} = 0\)
  - \(R\) = 1, \(S\) = 1: Not allowed

### JK Flip-Flop

- **Truth Table**
  - \(J\) = 0, \(K\) = 0: \(Q_{n+1} = Q_n\)
  - \(J\) = 0, \(K\) = 1: \(Q_{n+1} = 0\)
  - \(J\) = 1, \(K\) = 0: \(Q_{n+1} = 1\)
  - \(J\) = 1, \(K\) = 1: \(Q_{n+1} = \bar{Q}_n\)
The 555 timer

Astable Operation
For the following circuit:

\[
\text{thigh} = t_{low} = 1 \text{ms}
\]

A. Write KCL for node "a" in terms of \( V_I, V_L, R_1 \) and \( C_1 \).

\[
t_i = \frac{V_I}{R_1}, \quad \tau_i = C_i \frac{dV_I}{dt} \quad \therefore \quad \frac{V_I}{R_1} + C_i \frac{dV_I}{dt} = 0
\]

B. Derive an analytic expression for \( V_L(t) \) as a function of \( V_I(t) \) and the circuit parameters.

\[
a V_L = -\frac{1}{R_i C_i} \int V_I(\tau) d\tau
\]

C. Draw \( V_L(t) \) for the given input, label the amplitude and time.

\[
\text{amplitude} = \frac{1}{10^7}, \quad \text{time} = \frac{1}{10^7} \text{F}
\]

6.071 Final
D. Now consider the circuit

Note that the op-amp is used with positive feedback. Write down the state model for $V_2$ as a function of $V_{in}$

$$V_{in} = V_{inu} + \frac{i}{R_3}$$

$$i = \frac{V_{in} - V_{inu}}{R_3}$$

$$V_{in} = \frac{V_2 R_3 - V_{inu} R_3 + \sqrt{V_{inu} R_3 + V_{inu} R_3}}{R_3}$$

E. Draw the hysteresis loop and label all voltages.

F. Now combine the two circuits so that $V_1$ from U1 is the input to U2. Draw $V_1(t)$ and $V_2(t)$ on the plot below. Label all times and amplitudes.
Problem 2. (5 points)

Consider the transformer circuit.

For the ideal transformer $V_1 I_1 + V_2 I_2 = 0$ and $V_2 = nV_1$.

Calculate the Thévenin equivalent resistance looking into the port $V_1$.

\[
V_1 I_1 + V_L I_2 = 0 ;
\]

\[
\frac{I_1}{I_2} = -\frac{V_L}{V_1} = -n
\]

\[
I_2 = \frac{-I_1}{n}
\]

\[
V_L = \frac{-I_1 R_e}{n} \quad \text{and} \quad V_2 = \frac{-I_1 R_e}{n}
\]

\[
V_1 = \frac{V_2}{n} ; \quad V_1 = \frac{I_1 R_e}{n^2}
\]

\[
R_T = \frac{V_2}{I_1} = \frac{R_e}{n^2}
\]
Problem 3. (5 points)

Calculate the peak-to-peak voltage into a 50Ω resistor for a 20dBm sinusoid with a frequency of 1 MHz. (dBm is short for dB’s above 1 mW)

\[ 20 \text{dB} = 10 \log \frac{P_{\text{out}}}{1\text{mW}} \]

1. \[ P_{\text{out}} = 100 \text{ mW} = 0.1 \text{ W} \]

2. \[ P = \frac{V_{\text{rms}}^2}{R} \]
   \[ V_{\text{rms}} = \sqrt{5} \]
   \[ V_{p} = 2V_{\text{rms}} = 2\sqrt{5} \]
   \[ 2V_{p} = 2\sqrt{5} \]

\[ V_{pp} = 2V_{\text{rms}} \]
The switch in the circuit above was closed at a distant time (much larger than any transient) in the past.

A. With the switch still closed, what is the current through the inductor L1?

B. At time t=0 the switch is opened. Derive an expression for I(t).

\[ i(t) = \frac{V}{R_t} e^{-\left(\frac{R_t + R_x}{L}\right)t} \]
Problem 5. (10 points)

A. For each of the following filters identify them as: low pass, high pass, band pass, band reject.

B. Draw the frequency response of this filter made from an open-ended transmission line. The length, \( l_0 \), corresponds to a quarter wave length at 10 MHz. Draw \( \frac{V_{out}}{V_{in}}(f) \) for \( f = 0 \rightarrow 10 \text{ MHz} \)
Problem 6. (15 points)

For this circuit, the input voltage $V_{in}$ is from a digital circuit and can have only the 2 values: 4.2 V or 0.5 V. The transistor has $\beta=100$.

Calculate the output voltage for each of these voltages.

a) $V_{in} = 0.5$ V. $V_{out} =$ ?

$$V_{out} = \left( \frac{10k\Omega}{10.1k\Omega} \right) 10V$$

b) $V_{in} = 4.2$ V. $V_{out} =$ ?

$$V_e = 4.2 - 1.7V = 2.5V$$

$$I_e = \frac{3.5V}{24\Omega}$$

$$I_c = -I_e \therefore V_{out} = 10V - \left( \frac{3.5V}{24\Omega} \right) 100\Omega$$
The above operational amplifier uses a 6 V Zener diode to set V+ and it also uses negative feedback to generate a regulated Vout.

A. Calculate Vout

\[ V_+ = 6V \quad ; \quad V_- = 6V \]

\[ V_- = \left( \frac{10k\Omega}{15k\Omega} \right) V_{out} \quad ; \quad V_{in} = 6V \left( \frac{3}{5} \right) \]

\[ = 9V \]

B. What is the purpose of the 1kΩ resistor? (Note: this is NOT an example of positive feedback.)

\[ \text{To bring } \text{Zener} \]

\[ 6.071 \text{ Final} \quad \text{Page: 13} \]
Problem 8. (20 points)

You are tasked to design a security system for a long entrance hallway with doors on either end. The desired information is the number of people in the hallway at any given time. The system is set up so that people only move in one direction (left to right) and there are optical sensors on each opening to detect the passage of people through the openings.

\[ \text{d1} \quad \text{d2} \]

\( \text{d1} \) is a digital pulse which is high when a person moves through the left opening into the hallway, low otherwise.

\( \text{d2} \) is a digital pulse which is high when a person moves through the right opening out of the hallway, low otherwise.

Using flip-flops and digital logic we will design a system with 3 digital outputs (\( O_0, O_1, O_2 \)):

\( O_0 = \) High if people are in the hall, Low otherwise

\( O_1 = \) High if only one person is in the hall, Low otherwise

\( O_2 = \) High if only two people are in the hallway, Low otherwise.

Assume that there will never be more than two people at a time in the hallway. Also assume that initially there are no people in the hallway.

A. Based on the above rules, fill in the following timing diagram:

\[ \text{d1} \quad \text{d2} \]

\[ \text{o0} \quad \text{o1} \quad \text{o2} \]

6.071 Final
B. For the JK flip-flop arranged as follows,

![JK Flip-Flop Diagram]

Fill in the timing diagram below.

![Timing Diagram]

C. Guided by your answers to part A and B you are now in a position to design the complete system. Hint: The signals d1 and d2 at the entry and exit of the hallway are the trigger signals, similar to CLK of part B.

![Design Diagram]

Many other possible designs.