**Problem 1: The ADC0848**

a) Sketch a block diagram of the internal circuitry of the ADC and briefly explain what each block does.

A block diagram of the ADC0848 is shown below. The MUX is used to select between the 8 input channels either as single-ended or as differential. The address latch holds the selection code for this. The 8-bit Successive-Approximation (SAR) A/D block converts the signal to a binary representation where V\text{ref} is full scale. The output is fed into a set of tristate output latches which the control logic tells what to do. When the correct sequence of signals is sent, the results of the conversion are available at the output. When reading in data (for the address latch) the tri-state output is high impedance.

b) How many bits of precision, N, does the ADC0848 have?

N=8 for the ADC0848.

c) What is the smallest analog voltage change that causes the output digital code to change by 1 Least Significant Bit (LSB) of the converter? Express your answer in terms of the full-scale voltage $V_{FS}$ and N, and calculate a numerical value for the ADC0848 when $V_{FS} = 5V$.

The ADC divides its full scale voltage $V_{FS}$ into $2^N$ equal parts and assigns a digital code to each one. The smallest analog voltage change that causes the digital output to change by 1 LSB is thus $\frac{V_{FS}}{2^N}$. The ADC0848 has $N=8$; so if $V_{FS}=V_{REF}=5V$, the smallest analog voltage change it can detect is $\frac{5}{256} V = 19.5mV$.

d) What are the maximum and minimum values of $V_{FS}$ that can be used?
The full scale voltage of the ADC0848 is equal to the \( V_{\text{REF}} \), the voltage on pin 11. The maximum value of \( V_{\text{REF}} \) is limited to the supply voltage \( V_{\text{CC}} \), i.e. between 4.5V and 6V with a normal value of 5V. The minimum value of \( V_{\text{REF}} \) can be quite small, enabling accurate conversion of analog input signals with small ranges. However, both linearity and offset errors get worse as \( V_{\text{REF}} \) decreases (see figures from the data sheet below). This imposes practical lower limits on the minimum allowable \( V_{\text{REF}} \) for a given application.

Since offset error can always be calibrated out, linearity error is the real performance-limiting factor as \( V_{\text{REF}} \) decreases. If we allow a maximum linearity error of 0.5LSB, \( V_{\text{REF}} \) should be greater than about 0.2V. The smallest analog voltage change that can be detected by the ADC0848 with reasonable accuracy is thus \( \frac{0.2}{256} \cdot V = 0.78\text{mV} \).

e) What are the manufacturer’s specifications for the Integral Nonlinearity (INL) and Differential Nonlinearity (DNL) of the ADC0848?

The manufacturer (National Semiconductor) does not distinguish between INL and DNL on the data sheet, but lumps them together into a single performance specification called “linearity error”. This is guaranteed to be less than \( \pm1\text{ LSB} \) on average for the ADC0848CCN (the version we use in lab).

Problem 2: ADC Nomenclature

a) What do the terms "accuracy", "resolution", and "linearity" mean when applied to an ADC?

Accuracy is a measure of how close the converted value is to being the actual value. For example, if the input is 2V, the A/D should output the binary number representing 2V. The closer it is to 2V, the more accurate it is.

Resolution tells the smallest discernable input voltage difference the A/D can recognize. For the ADC0848, the resolution is \( V_{\text{ref}}/256 \) (19.5mV for a 5V reference). Any changes less than this will be seen as the same voltage.

Linearity describes how a linear equation can fit the relationship between input voltage and output number. Linearity is specified over the entire range of input voltages and measured by the maximum deviation from the ideal. If the input is stepped up with a given increment, the A/D should also step equally. Any deviation from this is called incremental or differential linearity (DNL) error.
b) The ADC0848 can make "ratiometric" conversions. What are these? What is the advantage of such a capability? To what extent will this capability affect the accuracy, resolution and linearity of the AD converter?

The ADC0848 data sheet describes a ratiometric system as one where “the analog input voltage is proportional to the voltage used in the A/D reference”. This reference potential is available to operate transducers as well as to supply the ADC. If the transducer output is proportional to the reference and the ADC output is proportional to the reference, then the value of the reference does not affect the conversion. Of course noise and dynamic range are affected. The ADC0848 can provide full resolution for references between about 0.2V and 5 volts. A separate regulated supply is often used.

**Problem 3: Implementing a Voltmeter**

a) Draw a schematic diagram (using OrCAD) of an interface between a DS5000 and an ADC0848CCN analog-to-digital converter which can initiate and read a conversion. Use PORT1.0 to initiate a conversion, PORT1.1 to sense if the converter is busy, and PORT1.3 to read data. Use PORT0 for the data bus.

An interface between the ADC0848 and DS5000 is shown below. Other details are not shown. PORT0 has no pull-up mechanism, so a 9X10K resistor array provides external pullups and allows data out. Digital and analog grounds are nominally at the same potential but are run separately. It is important to avoid transients and to minimize current flow in the analog ground path. Separate leads to a common (spatially close contacts with low contact resistance) point are useful when significant current flows in an analog ground line. 10 mA through 400 milliohms (two contacts) develops 4 mV drop!
b) Once you have drawn the proper connections, design a variable voltage source that uses a potentiometer and an amplifier circuit (the LMC6484 operational amplifier) to provide a test signal that spans the entire range of inputs for the ADC0848 but does not exceed its safe operating limits. To connect this variable voltage source to the ADC, use differential input mode, i.e. Channel 1 = V+ and Channel 2 = V-.

The variable voltage source is shown connected to Channel 1 of the ADC0848 in the figure above. The op-amp buffer ensures that the potentiometer voltage does not change because of the current drawn by the ADC input. In practice, the op-amp may not be needed since the ADC inputs only sink or source about 1 µA of current (i.e., the input impedance of the ADC channels is high compared to the resistance of the potentiometer).

c) Draw a graph that indicates the relationship between the input voltage and the output digital number for the ADC. The abscissa of the graph should represent the input voltage, and the ordinate should represent the digital number output by the ADC.

Ideally, this should be a staircase that approximates a straight line passing through the origin. In a real ADC the slope of the line will be incorrect (gain error) and it will not pass exactly through the origin (offset error). In addition, the input-output characteristic will not be precisely linear, resulting in INL and DNL error.