6.012 - Microelectronic Devices and Circuits
Lecture 8 - MOS Capacitors I - Outline

• Announcements
  Exam One - March 12, 54-100, 7:30 pm; past exams are posted on Stellar

• Review
  Wrapping up BJTs (for now)

• Qualitative description - MOS in thermal equilibrium
  Definition of structure: metal/silicon dioxide/p-type Si (Example: n-MOS)
  Electrostatic potential of metal relative to silicon: $\phi_m$
  Zero bias condition: Si surface depleted if $\phi_m > \phi_{p-Si}$ (typical situation)
  Negative bias on metal: depletion to flat-band to accumulation
  Positive bias on metal: depletion to threshold to inversion

• Quantitative modeling - MOS in thermal equilibrium, $V_{BC} = 0$
  Depletion approximation applied to the MOS capacitor:
  1. Flat-band voltage, $V_{FB}$
  2. Accumulation layer sheet charge density, $q_A^*$
  3. Maximum depletion region width, $X_{DT}$
  4. Threshold voltage, $V_T$
  5. Inversion layer sheet charge density, $q_N^*$
BJT Modeling: FAR models/characteristics

\[ \alpha_F = -\frac{i_C}{i_E} = \frac{1 - \delta_B}{1 + \delta_E} \approx \frac{1}{1 + \delta_E} \]

\[ \beta_F = \frac{i_C}{i_B} = \frac{1 - \delta_B}{\delta_E + \delta_B} \approx \frac{1}{\delta_E} \]

**Defects**

\[ \delta_E = \frac{D_h}{D_e} \cdot \frac{N_{AB}}{N_{DE}} \cdot \frac{w_{B,\text{eff}}}{w_{E,\text{eff}}} \]

\[ \delta_B \approx \frac{w_{B,\text{eff}}^2}{2L_{eB}^2} \]

**Design**

Doping: npn with \( N_{DE} \gg N_{AB} \)

\( w_{B,\text{eff}} \): very small

\( L_{eB} \): very large and \( \gg w_{B,\text{eff}} \)
BJT's, cont.: What about the collector doping, $N_{DC}$?
An effect we didn't put into our large signal model

- **Base width modulation** - the Early effect and Early voltage:
The width of the depletion region at the B-C junction increases as $v_{CE}$ increases and the effective base width, $w_{B,\text{eff}}$, gets smaller, thereby increasing $\beta$ and, in turn, $i_C$.

To minimize the Early effect we make $N_{DC} < N_{AB}$
- We will take this effect into account in our small signal LEC modeling.

- **Punch through** - base width modulation taken to the limit
When the depletion region at the B-C junction extends all the way through the base to the emitter, $I_C$ increases uncontrollably.
Punch through has a similar effect on the characteristics to that of reverse breakdown of the B-C junction.
pnp BJT's: The other "flavor" of bipolar junction transistor

Structure:

Symbol and FAR model:

Oriented with emitter down like npn:

Oriented as found in circuits:
Early Bipolar Junction Transistors - the first 10 yrs.

Alloy junction BJT - Early 1950's

Grown junction BJT - mid-1950's

Diffused junction BJT - late-1950's
**Integrated Bipolar Junction Transistors**

- integrated circuit processes.

Junction isolated integrated BJT - 1960's onward

Oxide isolated integrated BJT - a current process
Integrated circuit bipolar transistors: An early bipolar integrated circuit

A Fairchild Semiconductor DTL (digital) IC from 1964 (before most of us were born!)
Bipolar transistors in history: An early bipolar integrated circuit

Part of a series of US postage stamps commemorating the decade of the 1960's
IBM Oxide Isolated BJT with SiGe base

Color-enhanced cross-section photomicrograph

n-Channel MOSFET: Connecting with the npn MOSFET
A very similar behavior, and very similar uses.

MOSET

BJT

\[ i_D \approx K [v_{GS} - V_T(v_{BS})]^{2/2} \]

\[ i_B \approx I_{BSE} \frac{qV_{BE}}{kT} \]

\[ v_{CE} > 0.2 \text{ V} \]

\[ v_{BE} > 0.6 \text{ V} \]

\[ 0.2 \text{ V} \leq v_{CE} \]

\[ v_{BE} \leq 0.6 \text{ V} \]

\[ \beta_F i_B \]

Input curve

Output family
An n-channel MOSFET

In an n-channel MOSFET, we have two n-regions (the source and the drain), as in the npn BJT, with a p-region producing a potential barrier for electrons between them. In this device, however, it is the voltage on the gate, $v_{GS}$, that modulates the potential barrier height.

The heart of this device is the MOS capacitor, which we will study today. To analyze the MOS capacitor we will use the same depletion approximation that we introduced in conjunction with p-n junctions.
The n-MOS capacitor

Right: Basic device with $v_{BC} = 0$

Below: One-dimensional structure for depletion approximation analysis*

* Note: We can't forget the n+ region is there; we will need electrons, and they will come from there.
Electrostatic potential and net charge profiles

Zero bias: $v_{GB} = 0$

$\phi(x) = -t_{ox}$

$\phi_m$

$\phi_p$

$\rho(x) = q_{NA}x_d$

$q_{D^*} = -q_{NA}x_d$
Electrostatic potential and net charge profiles

Depletion: $V_{FB} < V_{GB} < 0$

$\phi(x) \quad \rho(x)$

$V_{FB} < V_{GB} < 0$

$\phi_m \quad \phi_p \quad \rho$
Electrostatic potential and net charge profiles

Flat band: $v_{GB} = V_{FB}$

$v_{GB} = V_{FB}$

$V_{FB} = \phi_p - \phi_m$

$V_{FB} = \phi_p - \phi_m$
Electrostatic potential and net charge profiles

Accumulation: $\nu_{GB} < \nu_{FB}$

\[ \phi(x) \]

\[ \rho(x) \]

$-t_{ox}$

$\nu_{GB} < \nu_{FB}$

$\phi_m$

$\phi_p$

$C_{ox}^*(\nu_{GB} - \nu_{FB})$

$-t_{ox}$

$-C_{ox}^*(\nu_{GB} - \nu_{FB})$
Electrostatic potential and net charge profiles

Flat band: $\nu_{GB} = V_{FB}$

$V_{FB} = \phi_p - \phi_m$

$\nu_{GB} = V_{FB}$
Electrostatic potential and net charge profiles

Depletion: $V_{FB} < V_{GB} < 0$

\[ \phi(x) = -t_{ox} + \int_{-qN_A}^{qN_A} \rho(x) \, dx \]

\[ V_{FB} < V_{GB} < 0 \]
Electrostatic potential and net charge profiles

Depletion: $v_{GB} = 0$

\[ \phi(x) = \phi_m - q_N A x \]

\[ \rho(x) = q_N A x_d \]

\[ q_D^* = -q_N A x_d \]
Electrostatic potential and net charge profiles

Depletion: $0 < v_{GB} < V_T$

$\phi(x)$

$0 < v_{GB} < V_T$

$x_d$

$\phi_m$

$\phi_p$

$-t_{ox}$

$qN_Ax_d$

$qD^* = -qN_Ax_d$

$J = 0 \Rightarrow n(x) = n_ie^{-q\phi(x)/kT}$

and $p(x) = n_ie^{q\phi(x)/kT}$

$\phi(0) \uparrow \Rightarrow n(0) \uparrow$
Electrostatic potential and net charge profiles

Threshold: $v_{GB} = V_T$

At threshold $\phi(0) = -\phi_p$

$\phi(0) = -\phi_p \Rightarrow n(0) = N_A$

$q_{D^*} = -qN_A X_{DT}$
Electrostatic potential and net charge profiles

Threshold*:

\[ v_{GB} = V_T \]

\[ X_{DT} = (2\varepsilon_S|2\phi_p|/q N_A)^{1/2} \]

\[ V_T - V_{FB} = |2\phi_p| + q N_A X_{DT}/C_{ox} \]

\[ V_T = V_{FB} + |2\phi_p| + (2\varepsilon_S|2\phi_p|q N_A)^{1/2}/C_{ox} \]

\[ q_{D^*} = -q N_A X_{DT} \]

\[ q_{D^*} = -(2\varepsilon_S|2\phi_p|q N_A)^{1/2} \]

* At threshold \( \phi(0) = -\phi_p \)
Electrostatic potential and net charge profiles

Inversion: $V_T < V_{GB}$

$\phi(x)$

$V_T < V_{GB}$

$-t_{ox}$

$-\phi_p$

$X_{DT}$

$|2\phi_p|$

$\phi_p$

$\phi_m$

$q_N^* = \text{Inversion layer charge}$

(sheet of mobile electrons in Si near the Si-oxide interface)

$q_{D^*} = -q_N^* (V_{GB} - V_T)$

$q_{D^*}$, depletion region charge unchanged

$q_{N^*} = -C_{ox^*} (V_{GB} - V_T)$

$q_{N^*} X_{DT} + C_{ox^*} (V_{GB} - V_T)$

$q_{D^*} = -q_N X_{DT}$

$\rho(x)$

$\phi(x)$
Electrostatic potential and net charge profiles - regions and boundaries

Accumulation
\( V_{GB} < V_{FB} \)

Depletion
\( V_{FB} < V_{GB} < V_T \)

Inversion
\( V_T < V_{GB} \)

Flat Band Voltage
\( V_{FB} = \phi_p - \phi_m \)

Threshold Voltage
\( V_T = V_{FB} + |2\phi_p| + (2\varepsilon_S|2\phi_p|qN_A)^{1/2}/C_{ox}^* \)
Electrostatic potential and net charge profiles
- the grand procession from accumulation to inversion -

Accumulation: \( v_{GB} < V_{FB} \)

\[ \phi_m = -C_{ox}^* (v_{GB} - V_{FB}) \]

\[ -t_{ox} \]

\[ \rho(x) \]

\[ \phi(x) \]

\[ -\phi_p \]

\[ -t_{ox} \]

\[ v_{GB} < V_{FB} \]

\[ V_T \]

\[ V_{FB} \]
Electrostatic potential and net charge profiles
- the grand procession from accumulation to inversion -

Flat band: \( V_{GB} = V_{FB} \)
Electrostatic potential and net charge profiles
- the grand procession from accumulation to inversion -

Depletion: $V_{FB} < V_{GB} < 0$

$V_T$

$V_{FB}$

$0$

$\phi(x)$

$\rho(x)$

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Electrostatic potential and net charge profiles
- the grand procession from accumulation to inversion -

Depletion: \( v_{\text{GB}} = 0 \)
Electrostatic potential and net charge profiles
- the grand procession from accumulation to inversion -

Depletion: $0 < v_{GB} < V_T$

\[\phi(x)\]

\[\rho(x)\]

\[qD^* = -qN_A x_d\]
Electrostatic potential and net charge profiles
- the grand procession from accumulation to inversion -

Threshold: $v_{GB} = V_T$

$V_T \leftarrow v_{GB} = V_T \rightarrow \phi(x)$

$qN_A X_{DT} \rightarrow \rho(x)$

$q_{D^*} = -qN_A X_{DT}$
Inversion: $V_T < V_{GB}$

Electrostatic potential and net charge profiles - the grand procession from accumulation to inversion -
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Lecture 8 - MOS Capacitors I - Summary

• Qualitative description
  Three surface conditions: accumulated, depleted, inverted
  Two key voltages: flat-band voltage, $V_{FB}$; threshold voltage, $V_T$
  The progression: accumulation through flat-band to depletion, then depletion through threshold to inversion

• Quantitative modeling
  Apply depletion approximation to the MOS capacitor, $v_{BC} = 0$
  Definitions: $V_{FB} \equiv v_{GB}$ such that $\phi(0) = \phi_{p-Si}$
  $V_T \equiv v_{GB}$ such that $\phi(0) = -\phi_{p-Si}$
  $C_{ox}^* \equiv \frac{\varepsilon_{ox}}{t_{ox}}$
  Results and expressions (For n-MOS example)
  1. Flat-band voltage, $V_{FB} = \phi_{p-Si} - \phi_m$
  2. Accumulation layer sheet charge density, $q_{A^*} = -C_{ox}^*(v_{GB} - V_{FB})$
  3. Maximum depletion region width, $X_{DT} = [2\varepsilon_{Si}|2\phi_{p-Si}|/qN_A]^{1/2}$
  4. Threshold voltage, $V_T = V_{FB} - 2\phi_{p-Si} + [2\varepsilon_{Si}qN_A|2\phi_{p-Si}|]^{1/2}/C_{ox}^*$
  5. Inversion layer sheet charge density, $q_{N^*} = -C_{ox}^*(v_{GB} - V_T)$