6.012 - Microelectronic Devices and Circuits
Lecture 21 - Diff-Amp Anal. I: Metrics, Max. Gain - Outline

• Announcements
  Announcements - D.P.: No Early effect in large signal analysis; just LECs.
  Do PS #10: free points while working on D.P.

• Review - Differential Amplifier Basics
  Difference- and common-mode signals: \( v_{ID} = v_{IN1} - v_{IN2}, \quad v_{IC} = \frac{v_{IN1} + v_{IN2}}{2} \)
  Half-circuits: half of original with wires shorted or cut (familiar, easy analyses)

• Performance metrics - specific to diff. amps.
  Difference- and common-mode gains
  Common-mode rejection ratio
  Input and output voltage swings

• Non-linear loads
  The limitation of resistive loads: Gain limited by voltage supply
  Non-linear loads: High incremental resistance/small voltage drop

• Active loads
  Lee load
  Current mirror load
**Differential Amplifiers** - overview of features and properties

**Intrinsic advantages and features:**
- large difference mode gain
- small common mode gain
- easy to cascade stages; no coupling capacitors
- no emitter/source capacitors in CS/CE stages

**Performance metrics:**
- difference mode voltage gain, $A_{vd}$
- common mode voltage gain, $A_{vc}$
- input resistance, $R_{in}$
- output resistance, $R_{out}$
- common mode input voltage range
- output voltage swing
- DC offset on output
- Power dissipation
Differential Amplifiers - common-mode input range

\((V_{C,\text{min}} \leq v_C \leq V_{C,\text{max}})\)

We have said the output changes very little for common-mode inputs. This is true as long as the \(v_C\) doesn't push the transistors out of saturation.

There are a minimum and maximum \(v_C\):

\(V_{C,\text{max}}\): As \(v_C\) increases, \(v_{SD9}\) decreases until \(Q_9\) is no longer in saturation.

\(V_{C,\text{min}}\): As \(v_C\) decreases, \(v_{DS10}\) and \(v_{DS11}\) decrease until \(Q_{10}\) and \(Q_{11}\) are no longer in saturation.

The node between \(Q_9\) and \(Q_{10}/Q_{11}\) moves up and down with \(v_C\).
Differential Amplifiers - output voltage range

\[ V_{\text{OUT,min}} \leq v_{\text{OUT}} \leq V_{\text{OUT,max}} \]

As \( v_{\text{OUT}} \) goes down, \( Q_{21}, Q_{23}, \) and/or \( Q_{25} \) may go out of saturation; as \( v_{\text{OUT}} \) goes up, the same may happen to \( Q_{17}, Q_{19}, \) and/or \( Q_{26}. \)
Differential Amplifier Analysis - 
incremental analysis exploiting symmetry and superposition

No voltage on common links, so incrementally they are grounded.

No current in common links, so incrementally they are open.
Looking at the design problem circuit:

Lesson - Draw the difference and common mode half circuits.

Voila!! We have reduced the transistor count from 29 to 4, and we see that our complex amplifier is a just cascade of 4 single-transistor stages.
Linear Resistor Loads:
the limit on maximum stage gain

- with linear resistor loads we must make a compromise between the voltage gain and the size of the output voltage swing.

Maximum voltage gains

\[
A_{v,\text{max}} = g_m R_{SL} \leq \frac{2 I_D R_{SL}}{V_{GS} - V_T} \leq \frac{2 \left[ I_D R_{SL} \right]_{\text{max}}}{\left[ V_{GS} - V_T \right]_{\text{min}}}
\]

**MOSFET**:

\[
V_{\text{in}} = V_{gs} 
\]

\[
V_{\text{out}} = g_m V_{gs} + g_o V_{out} + G_{SL} (\equiv 1/R_{SL})
\]

**Bipolar**:

\[
A_{v,\text{max}} = g_m R_{SL} = \frac{q I_C R_{SL}}{kT} \leq \frac{\left[ I_C R_{SL} \right]_{\text{max}}}{V_{\text{Thermal}}}
\]

What are \([I_C R_{SL}]_{\text{max}}, [I_D R_{SL}]_{\text{max}}, \text{ and } [V_{GS} - V_T]_{\text{min}}\) ?

* For a MOSFET, \(g_m = (2KI_D/\alpha)^{1/2} = K(V_{GS} - V_T)/\alpha = 2I_D/(V_{GS} - V_T)\)
Resistor Loads: cont.
- What are $[I_{DR_{SL}}]_{max}$, $[I_{CR_{SL}}]_{max}$, and $[V_{GS} - V_T]_{min}$?

$[I_{DR_{SL}}]_{max}$, $[I_{CR_{SL}}]_{max}$:
- $[I_{DR_{SL}}]_{max}$ and $[I_{CR_{SL}}]_{max}$ are determined by the desired voltage swing at the output and/or by the common-mode input voltage range.
- The ultimate limit is the power supply.

$[V_{GS} - V_T]_{min}$:
- $[V_{GS} - V_T]_{min}$ is set by how close to threshold the gate can safely be biased before the depletion approximation model fails. We will say more about this shortly (Slide 23).
Current Source Loads: Incrementally large resistance
Relatively small quiescent voltage drop
- transistors with a DC input voltage, i.e. set up as sources/sinks -

MOSFET:

\[
V_{REF}^+ \quad V_{REF}^- \quad V_{REF}^+ \quad V_{REF}^- \\
\]

\[
v_{gs} = 0 \quad G_m v_{gs} = 0 \quad G_{mb} v_{bs} = 0 \quad g_o = \lambda I_D = \frac{I_D}{V_A}
\]

Bipolar:

\[
V_{REF}^+ \quad V_{REF}^- \quad V_{REF}^+ \quad V_{REF}^- \\
\]

\[
v_{bs} = 0 \quad \pi = 0 \quad g_{\pi} = \lambda I_C = \frac{I_C}{V_A}
\]
**Current Source Loads:**

the limit on the maximum stage gain

- current source loads eliminate the need to compromise between the voltage gain and the output voltage swing

**Maximum voltage gains**

\[ A_{v,max} = \frac{g_m}{g_o + g_{sl}} = \frac{2I_D/[V_{GS} - V_T]}{I_D/V_{A,Q} + I_D/V_{A,SL}} \leq \frac{2V_{A,eff}}{[V_{GS} - V_T]_{\min}} \]

**MOSFET**: \[ g_m = (2KI_D/\alpha)^{1/2} = K(V_{GS} - V_T)/\alpha = 2I_D/(V_{GS} - V_T) \]

**Bipolar**: \[ A_{v,max} = \frac{g_m}{g_o + g_{sl}} = \frac{qI_C/kT}{I_C/V_{A,Q} + I_C/V_{A,SL}} = \frac{V_{A,eff}}{V_t} \]

with \[ V_{A,eff} = \frac{V_{A,Q}V_{A,SL}}{V_{A,Q} + V_{A,SL}}, \quad V_t = \frac{kT}{q} \]

Typically \[ V_{A,eff} >> [I_D R_{SL}]_{\max} \]
Current Source Loads: the maximum stage gain, cont.

- the similarity in the results for BJT's and MOSFETs operating in strong inversion extends to MOSFETs operating sub-threshold and in velocity saturation, also:

**Maximum voltage gains**

MOSFET sub-threshold: \[ i_D = I_{S,s-t} e^{(v_{GS} - V_T)/nV_t}, \quad g_m = \frac{I_D}{nV_t} \]

\[ |A_{v,\text{max}}| = \frac{g_m}{g_o + g_{sl}} = \frac{I_D/nV_t}{I_D/V_{A,Q} + I_D/V_{A,SL}} = \frac{V_{A,\text{eff}}}{nV_t} \]

MOSFET w. velocity saturation: \[ i_D = W s_{sat} C_{ox}^*(v_{GS} - V_T), \quad g_m = W s_{sat} C_{ox}^* = \frac{I_D}{(v_{GS} - V_T)} \]

\[ |A_{v,\text{max}}| = \frac{g_m}{g_o + g_{sl}} = \frac{I_D/(v_{GS} - V_T)}{I_D/V_{A,Q} + I_D/V_{A,SL}} \leq \frac{V_{A,\text{eff}}}{(v_{GS} - V_T)_{\text{min}}} \]

with \[ V_{A,\text{eff}} \equiv \frac{V_{A,Q} V_{A,SL}}{V_{A,Q} + V_{A,SL}} \]
Current Source Loads: Example - biasing a source-coupled pair differential amplifier stage

Want:

\[ \text{Note: } I_{\text{LOAD}} = I_{\text{BIAS}}/2 \]

Build:

\[ \text{Note: } W_1 = W_2 = W_3 \]
\[ W_7 = 2W_6 \]

This is nice...can we do even better?
Yes, with active loads. Consider...
**Active Loads:**

Loads that don't just sit there and look pretty.

First example: the current mirror load

Now "single ended," i.e. only one output, but it is twice as large:

\[ v_{out} = 2v_{out1} \]

Load self-adjusting; circuit forces

\[ I_{LOAD} = I_{BIAS}/2. \]
Active Loads: The current mirror load, cont.

Large differential-mode gain, small common-mode gain. Also provides high gain conversion from double-ended to single-ended output.

The circuit is no longer symmetrical, so half-circuit techniques cannot be applied. The full analysis is found in the course text. We find:

**Difference-mode inputs**

\[ v_{out,d} = \frac{2g_m}{g_o + g_{o2} + g_{el}} \frac{v_{id}}{2} \]
Active Loads: The current mirror load

**Common-mode inputs**

\[ v_{out,c} = \frac{g_{ob}}{2g_{m2}} v_{ic} \]

With both inputs:

\[ v_{out} = \frac{2g_{m3}}{(g_{o2} + g_{o4} + g_{el})} \left( \frac{v_{in1} - v_{in2}}{2} \right) - \frac{g_{ob}}{2g_{m2}} \left( \frac{v_{in1} + v_{in2}}{2} \right) \]

Note: In D.P. the output goes to the gate of a MOSFET; \( g_{el} = 0 \).
What if we want an active load and yet stay differential?

**Active Loads - The Lee load**

A load for a fully-differential stage that looks like a large resistance in difference-mode and small resistance in common-mode)

The conventional schematic is drawn here, but the coupling of the load and what is happening is made clearer by redrawing the circuit (next slide.)

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Clif Fonstad, 4/29/08
Active Loads - The Lee load. cont.

Drawn as on the right we see that the load MOSFETs on each side are driven by both outputs. The result is different if the two outputs are equal and opposite (diff-mode operation) or if they are equal (common-mode).

The next few slides give the results for each mode.

Drawn to highlight cross-coupling and demonstrate symmetry.
The Lee load: analysis for difference-mode inputs

LEHC: difference-mode

\[ v_{id}/2 = v_{gs5} \]

\[ g_{m5}v_{id}/2, g_{o5} \]

\[ g_{m1}v_{od}/2, g_{o1} \]

\[ -g_{m2}v_{od}/2, g_{o2} \]

\[ +v_{od}/2, g_{el} \]

\[ g_{oLLd} \]
The Lee load: analysis for difference-mode inputs, cont

**LEHC: difference-mode**

\[ \frac{v_{id}}{2} = v_{gs5} \]

\[ g_{m5} \frac{v_{id}}{2} \]

\[ g_{o5} \]

\[ g_{m1} \frac{v_{od}}{2} \]

\[ g_{o1} \]

\[ g_{o2} \]

\[ v_{od}/2 \]

\[ g_{el} \]

\[ \frac{v_{id}/2}{2} = v_{gs5} \]

\[ g_{m5} \frac{v_{id}/2}{2} \]

\[ g_{o5} \]

\[ g_{m1} \frac{v_{od}/2}{2} \]

\[ g_{o1} \]

\[ -g_{m2} \frac{v_{od}/2}{2} \]

\[ g_{o1} \]

\[ v_{od}/2 \]

\[ g_{el} \]

\[ g_{oLLd} = 2 \ g_{o1} \]

\[ A_{vd} = \frac{v_{od}}{v_{id}} = \frac{-g_{m5}}{g_{o5} + 2g_{o1} + g_{el}} \]

Note: In D.P., the outputs go to MOSFET gates so \( g_{el} = 0 \).
The Lee load: analysis for common-mode inputs

LEHC: common-mode
The Lee load: analysis for common-mode inputs, cont

LEHC: common-mode

\[ g_{oLLc} = 2(g_{m1} + g_{o1}) \approx 2g_{m1} \]

\[ A_{vc} = \frac{v_{oc}}{v_{ic}} = \frac{-g_{ob}}{2\left[2(g_{m1} + g_{o1}) + g_{el}\right]} \approx -\frac{g_{ob}}{4g_{m1}} \]

Note: In D.P., the outputs go to MOSFET gates so \( g_{el} = 0. \)
Achieving the maximum gain: Comparing linear resistors, current sources, and active loads

Maximum Gains

**MOSFET (SI)**

**Linear resistor loads**

$$\leq \frac{2[I_D R_{SL}]_{\text{max}}}{[V_{GS} - V_T]_{\text{min}}}$$

**Current source loads**

$$\leq \frac{2V_{A,\text{eff}}}{[V_{GS} - V_T]_{\text{min}}}$$

**Active loads**

**Difference mode**

$$\propto \frac{2V_{A,\text{eff}}}{[V_{GS} - V_T]_{\text{min}}}$$

**Common mode**

$$\propto \frac{2V_{A,\text{bias}}}{2V_{A,\text{bias}}}$$

**Bipolar-like**

*(BJT and Sub-$V_T$ MOS)*

$$\leq \frac{[I_C R_{SL}]_{\text{max}}}{n V_t}$$

Observations:

- Non-linear (current source) loads typically yield much higher gain than linear resistors, i.e. $V_{A,\text{eff}} \gg [I_D R_{SL}]_{\text{max}}$.
- The bias point is not as important to BJT-type stage gain.
- An SI MOSFET should be biased just above threshold for highest gain.
- For active loads what increases $A_{vd}$, decreases $A_{vc}$. 
Achieving the maximum gain: \((V_{GS}-V_T)_{\text{min}} = ?\)

For SI-MOSFETs, maximizing the voltage gain \(A_v\) or \(A_{vd}\) requires minimizing \(V_{GS}-V_T\). What is the limit?

Sub-threshold:

\[
\frac{A_v}{V_A} = \frac{1}{n V_t}
\]

Strong inversion:

\[
\frac{A_v}{V_A} = \frac{2}{(V_{GS}-V_T)}
\]

\(A_v/V_A\) is a smooth curve, so clearly \((V_{GS}-V_T)_{\text{min}} > 2nV_t\).

Note: \(n = 1.25\) was assumed.
Performance metrics - specific to diff. amps.

**Difference- and common-mode gains:** \( A_{vd} = \frac{v_{od}}{v_{id}} \), \( A_{vc} = \frac{v_{oc}}{v_{ic}} \)

**Common-mode rejection ratio:** \( CMRR = A_{vd}/A_{vc} \)

Common-mode input range

**Non-linear loads**

*Transistors biased in their constant current regions:*

- MOSFETs in saturation
- BJTs in their FAR

**Active loads**

*Current mirror load:*

Achieves double- to single-ended conversion without loss of gain
Has high resistance for difference-mode signals
Has low resistance for common-mode signals

*Lee Load:*

Maintains differential signals
Has high resistance for difference-mode signals
Has low resistance for common-mode signals