Lecture 24 - Final DP Issues; Intrin. Freq. Limits - Outline

• Announcements
  Stellar - Design Problem Foils; FAQs
  Design Problem - Due Friday, May 9 (tomorrow), by 5 pm in 13-3058*
  Final - Monday, May 19, 9:00 am - noon, Johnson Ice Rink

• DP Issues - DC Offset Voltage: \((v_{IN1} - v_{IN2})\) for \(v_{OUT} = 0\)
  Transfer characteristic of an op amp
  Looking at the individual stages
  Impact of DC offset voltage in op amp applications
  Cascodes with reduced offset

• Review - Dealing with shunting feedback capacitances: \(C_\mu\) and \(C_{gd}\)
  The Miller effect: any C bridging a gain stage looks bigger at the input
  The Marvelous cascode: CE/S-CB/G (E/SF-CB/G work, too - see \(\mu A741\))
  large bandwidth, large output resistance
  used in gain stages and in current sources
  Using the Miller effect to advantage: Stabilizing OP Amps - the \(\mu A741\)

• Intrinsic high frequency limits for transistors
  General approach

* and the Excel file on Stellar
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**D.C. Offset:** Looking at the amplifier transfer curve

**The concern:** \( v_{IN1} = v_{IN2} = 0 \) does not give \( v_{OUT} = 0 \)

Is this a problem?

First let's make sure we understand why there's an issue at all:

Everything goes up and down like we want, but the high impedance node is not at zero when the inputs are zero. It starts out at 0.8 or 0.9 Volts.
D.C. Offset, cont.: The amplifier transfer curve, cont.

As a result the overall amplifier transfer curve is offset from zero:

To start we can see where this characteristic and the offset come from by looking at the individual stage contributions.

* NOTE: The values of gain and the voltage levels on these foils are only approximate and vary depending on the design.
D.C. Offset, cont.: The individual stage transfer curves

The Lee Load Stage: The voltage swings are small and there is no offset or other issues here.

\[ v_{IN1} - v_{IN2} \text{ [µV]} \]

\[ -4.0 -3.0 -2.0 -1.0 \]

\[ v_{IN1} - v_{IN2} \text{ [µV]} \]

\[ 1.0 2.0 3.0 4.0 \]

* NOTE: The values of gain and the voltage levels on these foils are only approximate and vary depending on the design.
D.C. Offset, cont.: The individual stage transfer curves

The Follower Output Stage: The voltage swings here are large, but as long as we keep them in bounds things are fine; no offset either.

* NOTE: The values of gain and the voltage levels on these foils are only approximate and vary depending on the design.
The Current Mirror stage: Now we have a transfer curve that doesn't go through the origin, i.e. $v_{\text{OUT}} = 0.9 \, \text{V}$ for $v_{\text{IND}} = 0$; also, the voltage swings can push devices out of saturation.

**D.C. Offset, cont.:** The individual stage transfer curves

Note: The 130 $\mu\text{V}$ offset in the output of this stage corresponds to a 1.3 $\mu\text{V}$ offset at the op amp input. (More on next foil.)
**D.C. Offset, cont.:** Back to the original issue: the offset

The DC offset and where it can be seen: Is it a problem?

We always use op amps in feedback connections. In this type of connection the impact of the offset is negligible.

\[ v_{\text{OUT}} \approx 1.3 \mu V \]

\[ A_{vd} \approx -500,000 \]

Note: The offset for the D.P. op. amp. is \( v_{\text{OUT,CM}} \) when \( v_{\text{IN}} = 0 \) divided by the open circuit voltage gain. In our example, \( v_{\text{OUT,CM}} \) when \( v_{\text{IN}} = 0 \) is 0.9 V and \( A_{v,oc} = 700,000 \).
Output Stages: Push-pull or Totem Pole, cont.

Comments/Observations:
- The output resistance is largest around $v_{OUT} = 0$. Here both $Q_{28}$ and $Q_{29}$ are active and the output resistance is:
  $$ r_{out} \approx \frac{1}{g_{m28} + g_{m29}} $$
- One must always make $K_{28}/K_{24} = K_{29}/K_{27}$, and in the typical design $K_{24} = K_{27}$, and $K_{28} = K_{29}$. The bias current of $Q_{28}$ and $Q_{29}$ is set by $Q_{24}$ and $Q_{27}$:
  $$ I_{D28} = I_{D29} = \left(\frac{K_{28}}{K_{24}}\right)I_{D24} $$
- $|v_{OUT}|$ vs $|v_{IN}|$ is fairly linear over a wide range (see right); $|v_{GS}|$ increases slowly with $|v_{IN}|$.

NOTE: Graph plotted for a possible 2008 DP design.
**Design Problem Stage Gains:** Collecting what we know.

**Observation:** We have now found the voltage gain formulas for each of the three stages in the Design Problem. They are collected below:

**Lee Load gain stage:**

\[
\begin{align*}
v_{out1} &\approx \frac{-g_{m10}}{g_{o10} + 2g_{o12}} \frac{(v_{in1} - v_{in2})}{2} - \frac{g_{o9}}{4g_{m12}} \frac{(v_{in1} + v_{in2})}{2} \\
v_{out2} &\approx \frac{g_{m10}}{g_{o10} + 2g_{o12}} \frac{(v_{in1} - v_{in2})}{2} - \frac{g_{o9}}{4g_{m12}} \frac{(v_{in1} + v_{in2})}{2}
\end{align*}
\]

**Cascode current mirror gain stage:**

\[
\begin{align*}
v_{out} &\approx \frac{2g_{m23}}{g_{o17}g_{o19}/g_{m19} + g_{o23}g_{o21}/g_{m21}} \frac{(v_{in1} - v_{in2})}{2} - \frac{g_{m23}}{g_{m17}} \frac{(v_{in1} + v_{in2})}{2}
\end{align*}
\]

**Push-pull output stage:**

\[
v_{out} \approx \frac{R_L}{R_L + \frac{1}{2g_{m28}}} v_{in}
\]
Summary of **OCTC** and **SCTC** results

**OCTC**: an estimate for $\omega_{HI}$

1. $\omega_{HI}^*$ is a weighted sum of $\omega$'s associated with device capacitances: (add RC's and invert)
2. Smallest $\omega$ (largest RC) dominates $\omega_{HI}^*$
3. Provides a lower bound on $\omega_{HI}$

**SCTC**: an estimate for $\omega_{LO}$

1. $\omega_{LO}^*$ is a weighted sum of $\omega$'s associated with bias capacitors: (add $\omega$'s directly)
2. Largest $\omega$ (smallest RC) dominates $\omega_{LO}^*$
3. Provides a upper bound on $\omega_{LO}$
The Miller effect (general)

Consider an amplifier shunted by a capacitor, and consider how the capacitor looks at the input and output terminals:

\[ i_{in} = C_m \frac{d[(1 - A_v)v_{in}]}{dt} = (1 - A_v)C_m \frac{dv_{in}}{dt} \]

Note: \( A_v \) is negative

\[ C_m \frac{(1 - A_v)}{A_v} \approx C_m \]

\( C_{in} \) looks much bigger than \( C_m \)

\( C_{out} \) looks like \( C_m \)
The cascode when the substrate is grounded:
High frequency issues:

**L.E.C. of cascode:** can't use equivalent transistor idea here because it didn't address the issue of the C's!

Voltage gain ≈ -1 so minimal Miller effect.

Voltage gain ≈ \( g_m r_l \), without Miller effect.

Common-source gain without the Miller effect penalty!
Multi-stage amplifier analysis and design: The $\mu$A741

Figuring the circuit out:

- Emitter-follower/common-base "cascode" differential gain stage
- Darlington common-emitter gain stage
- Push-pull output
- Current mirror load

The full schematic

Simplified schematic
Multi-stage amplifier analysis and design: Two-port models

Representing our building-block stages:

\[ V_{in} \rightarrow \frac{g_m + g_{mb}}{g_m + g_{mb} + g_t} V_{in} \rightarrow V_{out} \]

Relative sizes:
- \( g_m, g_{mb} \): large
- \( g_o \): small
- \( g_t, g_l \): cannot generalize
Multi-stage amplifier analysis and design: Two-port models

Two different "cascode" configurations:

With MOSFETs, starting a cascode with a source follower costs a factor of two in gain, so it isn't very attractive.
Multi-stage amplifier analysis and design: Understanding the µA741 input "cascode"

Begin with the BJT building-block stages:

Relative sizes:
- $g_m$: large
- $g_{\pi}$: medium
- $g_o$: small
- $g_t, g_i$: cannot generalize
Multi-stage amplifier analysis and design: Two-port models

Two different "cascode" configurations, this time bipolar:

In a bipolar cascode, starting with an emitter follower still reduces the gain, but it also gives twice the input resistance, which is helpful.
Multi-stage amplifier analysis and design: The µA741

The chip: a bipolar IC first introduced in 1968 and still made today*

- Capacitor (this capacitor is what made the µA741 famous)
- Resistors
- Transistors
- Bonding pads
Multi-stage amplifier analysis and design: The µA741

The circuit: a full schematic

C₁ is in a Miller position across Q₁₆

The monolithic capacitor made the µA741 "complete" and a big success. Why is it needed? What does it do?
Multi-stage amplifier analysis and design: The µA741

Why is there a capacitor in the circuit?: the added capacitor introduces a low frequency pole that stabilizes the circuit.

Without it the gain is still greater than 1 when the phase shift exceeds 180° (dashed curve). This can result in positive feedback and instability.

With it the gain is less than 1 by the time the phase shift exceeds 180° (solid curve).
**Intrinsic performance - the best we can do**

We've focused on $\omega_{HI}$, the upper limit of mid-band, but even when $\omega > \omega_{HI}$ the $|A_v| > 1$, and the circuit is useful. For example, for the common source stage we had

$$A_v(j\omega) = \frac{-g_t\left(g_m - j\omega C_{gd}\right)}{\left((j\omega)^2 C_{gs} C_{gd} + j\omega\left[(g_l + g_o)C_{gs} + (g_l + g_o + g_t + g_m)C_{gd}\right] + (g_l + g_o)g_t\right)}$$

A Bode plot of $A_v$ is shown to the right:

When we look for a metric to compare the ultimate performance limits of transistors, we make note of this and ask how high can a device in isolation have provide voltage or current gain?
Intrinsic performance - the best we can do, cont.

Consider the two possibilities shown below, one for a voltage input and output where the metric would be the open circuit voltage gain, \( A_{v, oc} \), and the other for a current input and output with the metric being the short circuit current gain, \( A_{i, sc} \) (commonly written \( \beta_{sc} \)):

\[
A_{v, oc}(s) = \frac{v_{out}(j\omega)}{v_{in}(j\omega)} = \frac{g_m - j\omega C_{gd}}{g_o - j\omega C_{gd}}
\]

\[
\beta_{sc}(j\omega) = \frac{i_d(j\omega)}{i_s(j\omega)} = \frac{g_m - j\omega C_{gd}}{j\omega(C_{gs} + C_{gd})}
\]

Of these two alternatives, \( \beta_{sc} \) is the more useful. \( A_{v, oc} \) is derived with a voltage source driving a capacitor, something that doesn't give a meaningful result and leads to ever increasing input power. It also does not involve \( g_m \) and \( C_{gs} \). Consequently, short circuit current gain is used as the intrinsic high frequency performance metric for transistors.
Intrinsic high frequency limits for transistors

General approach: short-circuit current gains  (Lecture 25's topic; results below)

Limits for MOSFETs:

Metric - CS short-circuit current unity gain pt:  \( \omega_T = \frac{g_m}{[(C_{gs}+C_{gd})^2 - C_{gd}^2]^{1/2}} \)

\( \omega_T \) is approximately \( g_m/C_{gs} = 3\mu_e(V_{GS}-V_T)/2L^2 \)

\( g_m = (W/L)\mu_eC_{ox}^*(V_{GS}-V_T) \) and \( C_{gs} = (2/3)WLC_{ox}^* \)

so \( \omega_T \approx 3\mu_e(V_{GS}-V_T)/2L^2 = 1/\tau_{ch} \)

Design lessons: bias at large \( I_D \)
minimize \( L \)  \( \text{and } \)  \( L^2 \)
use n-channel rather than p-channel \( (\mu_e >> \mu_h) \)

Limits for BJTs:

Metrics - CE short-circuit current gain 3B pt:  \( \omega_b = \frac{g_p}{(C_{\pi} + C_{\mu})} \)

CE short-circuit current gain unit gain pt:  \( \omega_T = \frac{g_m}{(C_{\pi} + C_{\mu})} \)

\( \omega_T \) approaches 1/\( \tau_b \) as \( I_c \) increases and \( \tau_b = w_B^2/2D_{min,B} \)

so \( \omega_T \approx 2D_{min,B}/w_B^2 = 2\mu_eV_t/w_B^2 = 1/\tau_b \)

CB short-circuit current gain unit gain pt:  \( \omega_\alpha = \frac{g_m}{C_{\pi}} \)

Design lessons: bias at high collector current
minimize \( w_B \)  \( \text{and } \)  \( w_B^2 \)
use npn rather than pnp \( (\mu_e >> \mu_h) \)