Problem 1. Calculate the following using 6-bit 2’s complement arithmetic (which is just a fancy way of saying to do ordinary addition in base 2 keeping only 6 bits of your answer). Show your work using binary (base 2) notation. Remember that subtraction can be performed by negating the second operand and then adding it to the first operand.

\[
\begin{align*}
13 + 10 &= \quad 1011_2 + 1010_2 = \quad 10100_2 = 20 \\
15 - 18 &= \quad 1111_2 - 10000_2 = \quad 1111_2 = -3 \\
27 - 6 &= \quad 11011_2 - 0110_2 = \quad 10101_2 = 21 \\
-6 - 15 &= \quad 10110_2 - 11111_2 = \quad 11001_2 = -21 \\
21 + (-21) &= \quad 10101_2 + 11011_2 = \quad 100001_2 = 0 \\
31 + 12 &= \quad 11111_2 + 1100_2 = \quad 100101_2 = 45
\end{align*}
\]

Explain what happened in the last addition and in what sense your answer is "right".

Problem 2. Suppose we have two 2’s complement numbers, one of N bits and one of M bits (without loss of generality let N ≥ M). What is the minimum number of bits needed to represent the sum of the two numbers without any loss of information? What about the product of the two numbers?

Problem 3. Consider the following diagram of a simple sequential circuit:

The components labeled CL1 and CL2 are combinational; R1 and R2 are edge-triggered D registers. Timing parameters for component are as noted (we’re ignoring the registers’ hold time in this problem). Note that from the outside, the circuit looks behaves from a timing standpoint like a register: to ensure correct operation of the internal components,
the input IN must observe a setup time with respect to CLK, and that the output OUT is guaranteed to be stable with its new value some propagation delay after the rising edge of CLK.

(A) Write the timing specifications \( t_{\text{SETUP}}, t_{\text{PD}}, t_{\text{CLK}} \) for the system as a whole using the timing specifications for the internal components that are given in the figure. \( t_{\text{CLK}} \) is the minimum clock period for CLK that still ensures the circuit will work correctly (in particular, that the output of CL2 will meet the setup time for R2). Hint: refer to slide 16 of Lecture 14.

We've been treating wires as idealized components that introduce no delay of their own. In the real world, wires have resistance, capacitance and inductance that will cause different frequencies to propagate along the wire at different rates. This means that wires will delay the arrival of sharp rising and falling transitions (which you'll remember from Fourier analysis have signal components at many different frequencies). This effect is particularly bothersome in connection with clock signals since the clock may arrive at separate parts of the circuit at slightly different times. This difference in arrival times of the clock is called clock skew, which we'll model in our simple circuit above as explicit delays along each clock path:

![Diagram](image)

(B) Rewrite the timing specifications \( t_{\text{SETUP}} \) and \( t_{\text{PD}} \) for the system as a whole taking into account \( \delta_1 \) and \( \delta_2 \). Don’t make any assumptions about the relative sizes of the two delays.

(C) The relative clock skew \( (\delta_1-\delta_2) \) between two registers connected in a “pipeline” – where the output of the first register is connected, usually through logic, to the input of the second register – can also affect the design of a circuit. Explain how relative clock skew affects \( t_{\text{CLK}} \), the minimum period of CLK that still ensures the circuit will work correctly.
Problem 4. Consider the following combinational encryption device constructed from six modules:

The device takes an integer value, X, and computes an encrypted version C(X). In the diagram above, each combinational component is marked with its propagation delay in seconds; contamination delays are zero for each component.

In answering the following questions assume that registers added to the circuit introduce no additional delays (i.e., the registers have a propagation delay of zero, as well as zero setup and hold times). Any modifications must result in a circuit that obeys our rules for a well-formed pipeline and that computes the same results as the combinational circuit above. Remember that our pipeline convention requires that every pipeline stage to have a register on its output.

When answering the questions below, if you add a register to one of the arrows in the diagram, count it as a single register. For example, it takes two registers to pipeline both inputs to the rightmost module (the one with latency 4).

(A) What is the latency of the combinational encryption device?

(B) If we want to increase the throughput of the encryption device, what is the minimum number of registers we need to add? Explain.

(C) If we can add as many registers as we like, is there an upper bound on the throughput we can achieve? Explain.

(D) If we can add as many registers as we like, is there a lower bound on the latency we can achieve? Explain.