Introduction to Code Optimization
Instruction Scheduling
Outline

- Modern architectures
- Introduction to instruction scheduling
- List scheduling
- Resource constraints
- Scheduling across basic blocks
- Trace scheduling
Simple Machine Model

• Instructions are executed in sequence
  – Fetch, decode, execute, store results
  – One instruction at a time
• For branch instructions, start fetching from a different location if needed
  – Check branch condition
  – Next instruction may come from a new location given by the branch instruction
Simple Execution Model

- 5 Stage pipe-line

<table>
<thead>
<tr>
<th></th>
<th>fetch</th>
<th>decode</th>
<th>execute</th>
<th>memory</th>
<th>writeback</th>
</tr>
</thead>
</table>

- Fetch: get the next instruction
- Decode: figure-out what that instruction is
- Execute: Perform ALU operation
  - address calculation in a memory op
- Write Back: write the results back
Simple Execution Model

Inst 1

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**time**
Simple Execution Model
Outline

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From a Simple Machine Model to a Real Machine Model

• Many pipeline stages
  – Pentium 5
  – Pentium Pro 10
  – Pentium IV (130nm) 20
  – Pentium IV (90nm) 31
  – Core 2 Duo 14

• Different instructions taking different amount of time to execute

• Hardware to stall the pipeline if an instruction uses a result that is not ready
Real Machine Model cont.

• Most modern processors have multiple cores
  – Will deal with multicores next week
• Each core has multiple execution units (superscalar)
  – If the instruction sequence is correct, multiple operations will happen in the same cycles
  – Even more important to have the right instruction sequence
Instruction Scheduling

• Reorder instructions so that pipeline stalls are minimized
Constraints On Scheduling

• Data dependencies
• Control dependencies
• Resource Constraints
Data Dependency between Instructions

• If two instructions access the same variable, they can be dependent

• Kind of dependencies
  – True: write → read
  – Anti: read → write
  – Output: write → write

• What to do if two instructions are dependent.
  – The order of execution cannot be reversed
  – Reduce the possibilities for scheduling
Computing Dependencies

• For basic blocks, compute dependencies by walking through the instructions

• Identifying register dependencies is simple
  – is it the same register?

• For memory accesses
  – simple: base + offset1 \(\neq\) base + offset2
  – data dependence analysis: \(a[2i] \neq a[2i+1]\)
  – interprocedural analysis: global \(\neq\) parameter
  – pointer alias analysis: \(p1\rightarrow\text{foo} \neq p2\rightarrow\text{foo}\)
Representing Dependencies

- Using a dependence DAG, one per basic block
- Nodes are instructions, edges represent dependencies
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1: \( r2 = *(r1 + 4) \)
2: \( r3 = *(r1 + 8) \)
3: \( r4 = r2 + r3 \)
4: \( r5 = r2 - 1 \)
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• Edge is labeled with Latency:
  \( v(i \rightarrow j) = \text{delay required between initiation times of } i \text{ and } j \) minus the execution time required by \( i \)
Example

1: \( r2 = *(r1 + 4) \)
2: \( r3 = *(r2 + 4) \)
3: \( r4 = r2 + r3 \)
4: \( r5 = r2 - 1 \)
Another Example

1: \( r2 = *(r1 + 4) \)
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Control Dependencies and Resource Constraints

- For now, let's only worry about basic blocks
- For now, let's look at simple pipelines
Example

1: lea var_a, %rax
2: add $4, %rax
3: inc %r11
4: mov 4(%rsp), %r10
5: add %r10, 8(%rsp)
6: and 16(%rsp), %rbx
7: imul %rax, %rbx
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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# Example

<table>
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<tr>
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<tbody>
<tr>
<td>1</td>
<td>lea <code>var_a</code>, %rax</td>
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Example

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Outline

• Modern architectures
• Introduction to instruction scheduling
• List scheduling
• Resource constraints
• Scheduling across basic blocks
• Trace scheduling
List Scheduling Algorithm

• Idea
  – Do a topological sort of the dependence DAG
  – Consider when an instruction can be scheduled without causing a stall
  – Schedule the instruction if it causes no stall and all its predecessors are already scheduled

• Optimal list scheduling is NP-complete
  – Use heuristics when necessary
List Scheduling Algorithm

• Create a dependence DAG of a basic block
• Topological Sort
  READY = nodes with no predecessors
  Loop until READY is empty
    Schedule each node in READY when no stalling
  Update READY
Heuristics for selection

• Heuristics for selecting from the READY list
  – pick the node with the longest path to a leaf in the dependence graph
  – pick a node with most immediate successors
  – pick a node that can go to a less busy pipeline (in a superscalar)
Heuristics for selection

• pick the node with the longest path to a leaf in the dependence graph

• Algorithm (for node x)
  – If no successors \( d_x = 0 \)
  – \( d_x = \text{MAX}( d_y + c_{xy} ) \) for all successors y of x

  – reverse breadth-first visitation order
Heuristics for selection

- pick a node with most immediate successors
- Algorithm (for node x):
  - $f_x = \text{number of successors of } x$
### Example

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1: lea var_a, %rax
2: add $4, %rax
3: inc %r11
4: mov 4(%rsp), %r10
5: add %r10, 8(%rsp)
6: and 16(%rsp), %rbx
7: imul %rax, %rbx
8: mov %rbx, 16(%rsp)
9: lea var_b, %rax
Example

```
1  1  3  4
2  1  6  3
  1  4  3
  3  1  1
  7  8  9
4  3  5
```
Example

```
1 --- 7 --- 4  
 |     |     |  
1     d=0     d=0
2 --- 7 --- 5
 |     |     |  
1     4     d=0

7 --- 8 --- 9
 |     |     |  
3     d=0     d=0
```

$d=0$
Example

1

2

3

d=0

4

d=3

5

d=0

6

7

8

d=0

9

d=0

1

1

1

3

3

3

4

1

4

1

d=0

d=0
Example

```
1
 1
2
 1
 1
 3
 1
 4
 3
 5
 3
 3
 4
 1
 7
 3
 1
 8
 3
 9
 1
```

1 = d = 0
2 = d = 3
3 = d = 0
4 = d = 0
5 = d = 3
6 = d = 0
7 = d = 3
8 = d = 0
9 = d = 0
Example

\[ \begin{align*}
1 & \quad \text{d=0} \\
2 & \quad \text{d=3} \\
3 & \quad \text{d=0} \\
4 & \quad \text{d=3} \\
5 & \quad \text{d=0} \\
7 & \quad \text{d=3} \\
8 & \quad \text{d=0} \\
9 & \quad \text{d=0}
\end{align*} \]
Example

- Node 1: d=5, f=1
- Node 2: d=4, f=1
- Node 3: d=0, f=0
- Node 4: d=3, f=1
- Node 5: d=0, f=0
- Node 6: d=7, f=1
- Node 7: d=3, f=2
- Node 8: d=0, f=0
- Node 9: d=0, f=0

Connections:
- Node 1 to Node 2: d=1
- Node 2 to Node 7: d=1
- Node 2 to Node 8: d=3
- Node 3 to Node 7: d=4
- Node 4 to Node 7: d=3
- Node 5 to Node 7: d=1
- Node 6 to Node 7: d=7

Values:
- d: distance from the root
- f: feature value
READY = {{}}
Example

1, 3, 4, 6

READY = { }
Example

1, 3, 4, 6

READY = { 6, 1, 4, 3 }
Example

\[ \text{READY} = \{ 6, 1, 4, 3 \} \]
Example

READY = \{ 6, 1, 4, 3 \}
Example

READY = { 1, 4, 3 }
Example

READY = \{ 1, 4, 3 \}
Example

\[ \text{READY} = \{ 1, 4, 3 \} \]
Example

\[
\begin{align*}
&2 \\
\text{READY} &= \{4, 3\}
\end{align*}
\]
Example

READY = { 2, 4, 3 }
Example

READY = \{ 2, 4, 3 \}
READY = \{ 2, 4, 3 \}
Example

READY = \{ 2, 4, 3 \}
Example

7

READY = { 4, 3 }

1 → 2 → 7 → 8

3 → 6 → 7 → 9

4 → 5 → 7

d=5 f=1

d=4 f=1

d=3 f=2

d=3 f=0

d=0 f=0

d=0 f=0

f=0

f=0

f=0

f=0

f=0

f=0

f=0

f=1
Example

READY = \{ 7, 4, 3 \}
Example

READY = \{ 7, 4, 3 \}
READY = \{ 7, 4, 3 \}
Example

READY = \{ 7, 4, 3 \}
Example

$\text{READY} = \{ 7, 4, 3 \}$
Example

\[
\begin{align*}
\text{READY} &= \{ 7, 3 \} \\
5
\end{align*}
\]
Example

READY = \{ 7, 3, 5 \}
Example

\[
\text{READY} = \{7, 3, 5\}
\]
Example

READY = \{ 7, 3, 5 \}
Example

READY = \{ 7, 3, 5 \}
Example

8, 9
READY = \{ 3, 5 \}
Example

READY = \{ 3, 5, 8, 9 \}
Example

\[ \text{READY} = \{3, 5, 8, 9\} \]
Example

READY = \{ 3, 5, 8, 9 \}
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READY = \{ 5, 8, 9 \}
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READY = \{ 5, 8, 9 \}
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READY = \{ 5, 8, 9 \}
Example

\[ \text{READY} = \{5, 8, 9\} \]
Example

READY = { 8, 9 }
Example

READY = { 8, 9 }
Example

READY = { 8, 9 }
Example

READY = \{ 8, 9 \}
Example

READY = \{ 9 \}
Example

READY = \{ 9 \}
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READY = \{ 9 \}
Example

READY = \{ 9 \}
Example

$\text{READY} = \{\} \}$
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**9 cycles**
## Example

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14 cycles vs 9 cycles
Outline

• Modern architectures
• Introduction to instruction scheduling
• List scheduling
• Resource constraints
• Scheduling across basic blocks
• Trace scheduling
Resource Constraints

• Modern machines have many resource constraints

• Superscalar architectures:
  – can run few parallel operations
  – But have constraints
Resource Constraints of a Superscalar Processor

• Example:
  – One fully pipelined reg-to-reg unit
    • All integer operations taking one cycle
  In parallel with
  – One fully pipelined memory-to/from-reg unit
    • Data loads take two cycles
    • Data stores take one cycle
List Scheduling Algorithm with resource constraints

- Represent the superscalar architecture as multiple pipelines
  - Each pipeline represent some resource
List Scheduling Algorithm with resource constraints

• Represent the superscalar architecture as multiple pipelines
  – Each pipeline represent some resource

• Example
  – One single cycle reg-to-reg ALU unit
  – One two-cycle pipelined reg-to/from-memory unit
List Scheduling Algorithm with resource constraints

- Create a dependence DAG of a basic block
- Topological Sort
  
  READY = nodes with no predecessors

  Loop until READY is empty
  
  Let \( n \in \text{READY} \) be the node with the highest priority
  
  Schedule \( n \) in the earliest slot
  
  that satisfies precedence + resource constraints

  Update READY
Example

1: lea  var_a, %rax
2: add  4(%rsp), %rax
3: inc  %r11
4: mov  4(%rsp), %r10
5: mov  %r10, 8(%rsp)
6: and  $0x00ff, %rbx
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9: mov  %rbx, 16(%rsp)
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READY = { 1, 6, 4, 3 }
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ALUop

MEM 1

MEM 2
Example

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READY = { 1, 6, 4, 3 }

ALUop | 1 |       |       |       |       |
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READY = { 6, 4, 3 } ← 2
Example

1: lea  var_a, %rax
2: add  4(%rsp), %rax
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5: mov  %r10, 8(%rsp)
6: and  $0x00ff, %rbx
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READY = { 2, 6, 4, 3 }

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`READY = { 2, 6, 4, 3 }`
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READY = { 2, 6, 4, 3 }

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READY = { 6, 4, 3 }

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READY = { 4, 3 } ← 7

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READY = { 4, 7, 3 }

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READY = { 4, 7, 3 }

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READY = { 7, 3 } ← 5

ALUop | 1 | 6 |   |   |   |   |
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MEM 2  | 4 | 2 |   |   |   |   |
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READY = { 7, 3, 5 }
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READY = { 7, 3, 5 }

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READY = { 3, 5 } ← 8, 9
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READY = { 8, 9 }

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7: imul %rax, %rbx
8: lea var_b, %rax
9: mov %rbx, 16(%rsp)

READY = { }
Outline

• Modern architectures
• Introduction to instruction scheduling
• List scheduling
• Resource constraints
• Scheduling across basic blocks
• Trace scheduling
Scheduling across basic blocks

- Number of instructions in a basic block is small
  - Cannot keep a multiple units with long pipelines busy by just scheduling within a basic block
- Need to handle control dependence
  - Scheduling constraints across basic blocks
  - Scheduling policy
Moving across basic blocks

- Downward to adjacent basic block
Moving across basic blocks

- Downward to adjacent basic block
Moving across basic blocks

- Downward to adjacent basic block

A

B C

- A path to B that does not execute A?
Moving across basic blocks

- Upward to adjacent basic block
Moving across basic blocks

- Upward to adjacent basic block
Moving across basic blocks

- Upward to adjacent basic block

- A path from C that does not reach A?
Control Dependencies

• Constraints in moving instructions across basic blocks
Control Dependencies

• Constraints in moving instructions across basic blocks

\[
\text{if ( . . . )} \quad a = b \ \text{op} \ c
\]
Control Dependencies

• Constraints in moving instructions across basic blocks

```plaintext
if ( . . . )
  a = b op c
```
Control Dependencies

• Constraints in moving instructions across basic blocks

```c
if ( c != 0 )
a = b / c
```

*NO!!!*
Control Dependencies

• Constraints in moving instructions across basic blocks

\[
\text{If ( . . . )}
\]
\[
d = *(a1)
\]
Control Dependencies

• Constraints in moving instructions across basic blocks

\[ \text{If ( valid address? )} \]
\[ d = *(a1) \]
Outline

- Modern architectures
- Introduction to instruction scheduling
- List scheduling
- Resource constraints
- Scheduling across basic blocks
- Trace scheduling
Trace Scheduling

• Find the most common trace of basic blocks
  – Use profile information

• Combine the basic blocks in the trace and schedule them as one block

• Create clean-up code if the execution goes off-trace
Trace Scheduling

A

B

C

D

E

F

G

H
Trace Scheduling

A

B

C

D

E

F

G

H
Trace Scheduling

A

B

D

E

G

H
Trace Scheduling

A → B → D → E → G → H
Trace Scheduling

A → B → D → E → G → H
Large Basic Blocks via Code Duplication

• Creating large extended basic blocks by duplication
• Schedule the larger blocks
Large Basic Blocks via Code Duplication

- Creating large extended basic blocks by duplication
- Schedule the larger blocks
Trace Scheduling

A

B

D

E

G

H
Trace Scheduling
Next

• Scheduling for loops
• Loop unrolling
• Software pipelining
• Interaction with register allocation
• Hardware vs. Compiler