Lecture 6 - Epitaxy; M-S Junctions - Outline

• **Epitaxy and Strain**
  - Epitaxy practice: 1. LPE, 2. CVD (Halide and MO), 3. MBE
  - Pseudomorphic and metamorphic layers

• **Metal-Semiconductor Junctions in TE**  
  (Establishing the baseline)
  - Ideal junction - no surface states
  - Real junctions - surface states and Fermi level pinning

• **MS Junctions with bias (i-v and c-v)**  
  (Where it gets interesting, i.e. useful)
  - Forward bias, current flow
    1. General comments; 2. Thermionic emission theory;
    3. Drift-diffusion theory; 4. Real junctions
  - Reverse bias, image-force lowering
  - Switching dynamics
    1. Step response; 2. High frequency response

• **Applications**  
  (Benefiting from these simple structures)
  - Ohmic contacts
  - Doping profiling
  - Shunt diodes
  - UV photodiodes
  - FET gate (MESFETs)
Lattice-matched epilayers - substrate provides perfect template

Bulk substrate and epi material

Perfectly lattice-matched epilayer

Substrate
III-V systems: InGaAsP and AlGaAs
Mis-matched epilayers - strained to conform:

“pseudomorphic”

Bulk substrate and epi material

Strained “Pseudomorphic” Epilayer

Substrate
Impact of uniaxial strain on bands - bands shift removing $\Gamma$ degeneracy and changing band gaps

Tensile strain in growth plane (growth on larger lattice substrate)

Unstrained (growth on lattice matched substrate)

Compressive strain in growth plane (growth on smaller lattice substrate)

After Singh EOPSS Fig. 3.15
Critical layer thicknesses - Two classical models

People-Bean model vs. Matthews-Blakeslee model

The former was developed for, and is more relevant to, Si-Ge.
The later is more relevant to III-V epitaxy.

Adapted from Figure 7.8 from Molecular Beam Epitaxy by M. A. Herman and H. Sitter (Springer, 1996) ISBN 3-540-60594-0; QC611.6.M64H47 1966
Critical layer thicknesses - an important observation

The relevant critical thickness depends on the property/feature of interest
(work of Professor Jesus del Alamo and Jagdeep Bahl, MIT)
Mis-matched epilayers - relaxed: “metamorphic”

Fully relaxed “Metamorphic” Epilayer

Strained “Pseudomorphic” Epilayer

Substrate

Note: The transition from strained to relaxed is never so abrupt and typically occurs over many lattice periods.
Metamorphic layer growth - defect reduction, step grading

Each step is thick enough that relaxation occurs before the next step begins.

Ga$_{0.8}$In$_{0.2}$As (relaxed metamorphic layer)

Ga$_{0.84}$In$_{0.16}$As
Ga$_{0.88}$In$_{0.12}$As
Ga$_{0.92}$In$_{0.08}$As
Ga$_{0.96}$In$_{0.04}$As

GaAs (substrate)
Metamorphic layer growth - defect reduction, linear grading

The ramp is slow enough that the growing layer is 80-90% relaxed. The overshoot is designed to result in a fully-relaxed metamorphic layer.
There is no general agreement on which approach is superior and the choice often one of convenience and/or practicality. Because the last layer is often not fully relaxed, it is common to grade to a certain level and then step back, as seen in the structure on the left. In this way a fully relaxed top structure can be realized.

Note: Relaxed mismatched layers are termed "metamorphic". Strained mismatched layers are called "pseudomorphic"
Liquid Phase Epitaxy - LPE
Growth from a Ga or In solution in a hydrogen ambient

Exploded view of an LPE boat

Material:
Machined pyrolytic graphite

Ambient:
Purified hydrogen at atmospheric pressure within a quartz tube in a resistance heated furnace

Advantages: Near-equilibrium growth, excellent crystal quality
Inexpensive; Fast

Disadvantages: Difficult to scale up for production
Dimensional control poor
Structure complexity limited

Current status: Widely used for LEDs and laser diodes in well established processes. Rarely used in new installations.
As $T$ is reduced the binary (or ternary) solidifies from the melt:

- In the case of the binary shown on the left the liquid is $\text{In}_{1-x}P_x$, and the solid is $\text{InP}$.

- In the case of the ternary shown on the right, the situation is more complicated, because the liquid is $A_yB_zC_{1-y-z}$ and the solid is $A_xB_{1-x}C$, so the relationship between the liquid composition and $x$ is also needed. This information for cases of interest are in the literature.

Chlorine Transport Vapor Phase Epitaxy - VPE

GaCl$_3$ + AsH$_3$ $\rightarrow$ GaAs + 3HCl

**Advantages:** Conceptually simple; fast growth rate  
(good for thick epi)

**Disadvantages:** Messy  
Difficult to control group III supply  
Uses toxic gases (AsH$_3$, PH$_3$)

**Current status:** Used for some GaAs epitaxy where high purity  
(low background doping) needed, and for very thick layers; largely superceded by MOCVD
Metalorganic Chemical Vapor Deposition - MOCVD

Group III elements transported as a metalorganic compound on a carrier gas:

i.e.

$\text{Ga(CH}_3\text{)}_3 + \text{AsH}_3 \rightarrow \text{GaAs} + 3\text{CH}_4$

**Advantages:**
- All sources gaseous
- Precise composition and dimension control

**Disadvantages:**
- Involves complex chemistry
- Uses toxic gases ($\text{AsH}_3$, $\text{PH}_3$)

**Current status:** Viewed as the standard production process for many epitaxial heterostructures
Metalorganic Chemical Vapor Deposition - MOCVD

A group III precursor bubbler:

**Operation:**

- Bubbler held in constant-temperature bath
- Hydrogen "carrier" saturated with precursor (group III metalorganic) at fixed T
- Precursor transported through heated lines as a "gas"
- Flow controlled by mass flow meters

Figure from Rohm and Hass Metalorganics website: www.metalorganics.com
Molecular Beam Epitaxy - MBE

Slow vacuum deposition on a heated substrate under ultra-high vacuum conditions; growth a layer at a time

+': Extremely flexible, simple chemistry
    - Insitu monitoring; Atomic layer control
    - Non-equilibrium technique

-': No in situ cleaning or purifying reactions
    - Expensive (to assemble and operate)
    - Non-equilibrium technique

Status: A research workhorse; increasingly used heavily in production
Solid source molecular beam epitaxy system (NTU)

**UHV System**

Base pressure: $10^{-11}$ Torr (with cryogenic cooling)
Pressure during epitaxial growth: $10^{-8}$ to $10^{-7}$ Torr

**Element Sources**

- Al, Ga, In: effusion cells
- P, As, Sb: valved crackers
- N: radio frequency $\text{N}_2$ plasma source, or $\text{NH}_3$ cracker

_Courtesy Prof. Yoon Soon Fatt, NTU_
**In-situ monitoring of monolayer growth**

Reflection high energy electron diffraction (RHEED) pattern of a GaAs surface observed during epitaxial growth under As over-pressure conditions.

Specular reflection indicates surface reconstruction.

Intensity of straight-through beam fluctuates from low to high as each new monolayer forms.

Courtesy Prof. Yoon Soon Fatt, NTU
Variations on the MBE theme

**Solid Source MBE** - all elemental sources

*Advantages:* no toxic gases
*Disadvantages:* large heat load; phosphides require cracker or sublimation source

**Gas Source MBE** - column V hydrides; elemental group III's

*Advantages:* easy access to phosphides; no As or P cells to recharge
*Disadvantages:* large heat load; toxic gases; additional pump load

**Metalorganic MBE** - column III metalorganics; elemental V's

*Advantages:* reduced heat load
*Disadvantages:* phosphides difficult; MO purity an issue; carbon contamination a concern; additional pumping load; little advantage over SSMBE; more complex chemistry

**Chemical Beam Epitaxy** - MOCVD in high vacuum, beam limit

*Advantages:* small heat load; phosphides easy; selective area growth possible
*Disadvantages:* additional pumping load; carbon contamination possible; MO purity an issue; toxic gases
Critiquing the Epitaxy Techniques

**Liquid Phase Epitaxy**

**Advantages:** inexpensive; equilibrium growth; excellent layer quality; low toxicity
**Disadvantages:** complicated to do multiple layers; poor thickness control; materials and combinations limited; uniformity an issue; hard to scale up

**Vapor Phase Epitaxy** [chloride and hydride transport]

**Advantages:** high purity; low toxicity; high growth rate
**Disadvantages:** complex, messy; memory effects; poor thickness control; uniformity an issue

**Metalorganic Chemical Vapor Deposition** [esp. low P]

**Advantages:** excellent control; fast response; versatile; many materials; selective area growth possible
**Disadvantages:** toxic gases; uniformity an issue

**Molecular beam epitaxy**

**Advantages:** beam technique; in situ monitoring; monolayer control
**Disadvantages:** slow; expensive; maintenance of UHV required
Epitaxial growth techniques

- **Molecular Beam Epitaxy (MBE)**
  - Ultra high vacuum condition
  - Solid source MBE – Elemental sources of In, Ga, Al, As and P
  - Gas source MBE – Combination of elemental source (for group III) and gas source (for group V)

- **Metalorganic Chemical Vapor Deposition (MOCVD)**
  - Low vacuum condition
  - Gas sources such as TMG, TMI, TMA, AsH$_3$ and PH$_3$ are used.

*Courtesy of MBE Technology (S) Pte Ltd*
Final comments - What's hot in epi today...

AlGaInN on whatever: substrates are the problem
  Sapphire (Al$_2$O$_3$), Silicon Carbide (SiC)
  Gallium Nitride - if available
  Si - <111> best

InGaAs on GaAs and GaInAsN on GaAs: getting longer wavelengths, higher mobilities on an inexpensive substrate (rather than on InP)

Strained and unstrained Si-Ge-C layers on Si: to get higher hole and electron mobilities

Quantum dots: looking for improved optical properties, including direct transitions in group IV compounds

GaAs and InP on Si: dealing with 1. lattice mismatch, 2. anti-phase domains, and 3. thermal expansion coefficients; current interest in growing on Ge on Si
III-V Processing - General Comments/Overview

General Picture
III-V device processing is in general more complex than silicon processing in that
1. there are no native oxides comparable to SiO₂
2. many of the constituent elements in the III-V semiconductors have high vapor pressures and are subject to decomposition unless encapsulated or under pressure

On the other hand, with the III-Vs
1. one has the availability of complex heterostructures
2. there are very selective etches available to differentiate between heterostructure components
III-V Processing - General Comments, cont.

**Doping**
- diffusion: open tube (a la Si) not practical
- sealed ampoule - to provide As or P overpres.
- from spin-on glasses and doped metals
- ion implantation: standard process w. RTA activation
- direct growth: doped layers grown in desired profile

**Device isolation**
- mesa etching
- proton (H\(^+\)) bombardment: makes many wider bandgap
  III-V's like GaAs, InP high resistance

**Passivation, encapsulation**
- no native oxides; oxidation not viable - sulfidation maybe;
- deposited SiO\(_2\) and Si\(_3\)N\(_4\) widely used - Ga diffuses thru
  SiO\(_2\), but not Si\(_3\)N\(_4\)
III-V Processing - General Comments, cont.

**Ohmic contacts**

deposition and alloy of doped metals - e.g. Au-Zn
narrow bandgap ohmic contact layer - e.g. InGaAs
heavily doped layer contact layer - Si standard too.

**Wet etching**

there are highly selective etches for III-V hetero-structures that can be used to advantage in device processing:

Etchants that differentiate between AlGaAs and AlAs, or between GaAs and AlGaAs for selected AlGaAs aluminum fraction ranges
Similar etchants in the InGaAlAs system
Etchants that differentiate between InGaAlAs and InP

**Dry etching**

widely employed
Metal-Semiconductor Junctions - the structure

The structure is very simple

This is the "junction" we're talking about

but also very interesting, important, and useful
Metal-Semiconductor Junctions - barrier basics

- The evolution of the electrostatic barrier at the interface
  Initially we assume no surface states, i.e. bulk bands right to surface

- The energy band picture in isolation
  An isolated metal and an isolated semiconductor; neither "sees" the other

\[ q\Phi_m = q\chi_s + kT \ln \left( \frac{N_C}{N_D} \right) \]

The vacuum reference levels are equal.
Both materials are neutral.
Note definitions of \( \phi \) (work function) and \( \chi \) (electron affinity)

Note: no surface states for now; they come later
Metal-Semiconductor Junctions - barrier basics

- The metal and semiconductor shorted electrically
  
  The short imposes a constant Fermi level throughout

The combination remains neutral, but the two materials become charged as electrons flow from the semiconductor to the metal until the Fermi levels are the same. The semiconductor surface is slightly depleted at large separation; the depletion increases as they approach.
Metal-Semiconductor Junctions - barrier basics

- Shorted metal and semiconductor in physical contact
  As the distance between the metal and semiconductor decreases to zero, the depletion region grows.

The final depletion region width is that needed to support a potential change equal to the built-in potential, $\phi_b (= \phi_m - \phi_s)$.

The total structure is neutral, but there is now a dipole layer between the metal and semiconductor.
To model this we use the depletion approximation.
Metal-Semiconductor Junctions - progression of the barrier with decreasing separation

- 200 nm
- 100 nm
- 50 nm
- 1 nm
Metal-Semiconductor Junctions - barrier basics

- Depletion approximation

The charge in the metal is approximated as a sheet (impulse) charge density at the surface, and charge in the semiconductor is approximated by a fully depleted layer $X_D$ wide:

\[
\rho(x) \sim \begin{cases} 
Q^* \delta(x) & \text{for } x \leq 0 \\ 
qN_D & \text{for } 0 < x \leq X_D \\ 
0 & \text{for } X_D < x 
\end{cases}
\]

Charge neutrality requires $Q^* = -qN_DX_D$.

Remember we are dealing with sheet charge density, Coul/cm$^2$. 

Fonstad/Palacios 2/24/09
Depletion approximation (cont)

Integrating the charge divided by the dielectric constant yields the electric field

\[ E(x) = \int \left[ \frac{\rho(x)}{\varepsilon} \right] \, dx \]

We get:

\[ E(x) \approx \begin{cases} 
0 & \text{for } x \leq 0 \\
qN_D \frac{(x - X_D)}{\varepsilon} & \text{for } 0 < x \leq X_D \\
0 & \text{for } X_D < x 
\end{cases} \]
• Depletion approximation (cont)

Integrating the electric field yields the electrostatic potential

\[ \phi(x) = - \int E(x) \, dx \]

We get:

\[ \phi(x) \approx \begin{cases} 
\phi_b & \text{for } x \leq 0 \\
qN_D(x - x_d)^2/2\varepsilon & \text{for } 0 < x \leq x_d \\
0 & \text{for } x_d < x 
\end{cases} \]

Requiring that \( \phi(x) \) be continuous at \( x = 0 \) we find that the depletion region width, \( X_D \), must be

\[ X_D \approx \left( \frac{2\varepsilon \phi_b}{qN_D} \right)^{1/2} \]

The profile is now fully determined. (i.e., we're done)
Real semiconductor surfaces - surface states

• Surface states

There will be additional energy states on the surface of a semiconductor because the perfectly periodic lattice ends at the surface and many bonds are not "satisfied"
These states... can have a very high density
have a narrow distribution of energies within bandgap

• The energy bands in a semiconductor with surface states

The surface states typically are sufficiently dense that in equilibrium the Fermi level falls within them at the surface and the surface is depleted:

\[ q\phi_{sd} = fE_g - kT \ln(N_C/N_D) \]

Note: 0 < f < 1; for many III-V’s f ≈ 0.6-0.7
Real semiconductor surfaces - surface states, cont.

• Estimating the number of surface states
  Unit cell 5.5Å by 5.5Å → 3 \times 10^{14} \text{ cells/cm}^2 \text{ at surface}
  4 unsatisfied bonds per cell → \approx 10^{15} \text{ states/cm}^2
  If the states fall within 0.1 eV of each other → \approx 10^{16} \text{ states/cm}^2-eV
  This is very large!!

• What does this mean as a practical matter?
  Suppose \( \phi_m - \chi_s = 0.5 \) V, and that the effective separation of the charge in the surface states and metal is 25nm. The sheet charge density induced in this situation is:
    \[ Q^* = \varepsilon \Delta V/d = 10^{-12} \times 0.5 / 2.5 \times 10^{-6} = 2 \times 10^{-6} \text{ coul/cm}^2 \]
  The corresponding state density is \( Q^*/q \approx 10^{13} \text{ cm}^{-2} \)

  If all the surface states are active, the Fermi level at the surface will change only 1 mV; if only 10% are active it is only 10 mV. Only if 1%, or less, are active can the surface be unpinned.

• Conclusion
  The metal work function is often not the main determinant of the potential barrier in a metal-semiconductor junction.
Metal-Semiconductor Junctions - w. surface states

- The energy band picture in isolation with surface states

The surface of the semiconductor is depleted because of the charged surface states, independent of there being any metal nearby.

\[
q \Phi_m = f E_g, \quad q \chi_s
\]

\[
q \phi_{sd} = f E_g - kT \ln(N_C/N_D)
\]

Note: \(0 < f < 1\); for many III-V's \(f \approx 0.6-0.7\)
Metal-Semiconductor Junctions - w. surface states (cont.)

- Shorted metal and semiconductor, with surface states, in physical contact

When the density of surface states is high, as it typically is, the potential barrier that develops is dominated by the location of the surface states in the semiconductor band gap, rather than by the work function of the metal.

Otherwise, nothing is different and the same modeling holds.
Barrier heights

vs.

metal work function

- the impact of surface states on metal-semiconductor barrier heights

\[ \phi_{Bn} = 0.27\phi_m - 0.55 \]

(c2 = 0.27)

- the barrier height varies much less than does the work function of the metal

Sze PSD Chap 8, Fig 7

Sze PSD Chap 8, Fig 8
Applying bias to a metal-semiconductor junction

- What happens globally
  Potential step crossing junction changes
  Depletion region width and electric field change
  Current flows across junction

- Potential step change

  **Reverse bias**
  $qV_{AB}$
  $q(\phi_b - V_{AB})$

  **Forward bias**
  $qV_{AB}$
  $q(\phi_b - V_{AB})$

Assuming all the bias appears across the junction, the potential barrier changes from $\phi_b$ to $\phi_b - V_{AB}$

$\phi_b \longrightarrow \phi_b - V_{AB}$

**Note:** Forward bias decreases the barrier
Reverse bias increases the barrier
Applying bias to a metal-semiconductor junction, cont.

- Depletion region width and field changes

  Wherever $\phi_b$ appears in the expressions for depletion region width and electric field, it is replaced by $\phi_b - v_{AB}$:

  **Depletion region width:**
  \[
  X_D \rightarrow \left[ \frac{2\varepsilon (\phi_b - v_{AB})}{qN_D} \right]^{1/2}
  \]

  Note: The depletion region width decreases in forward bias. Reverse bias increases the depletion region width.

  **Peak electric field:**
  \[
  E_{pk} = \left[ \frac{2\varepsilon \phi_b qN_D}{\varepsilon} \right]^{1/2} \rightarrow \left[ \frac{2\varepsilon (\phi_b - v_{AB}) qN_D}{\varepsilon} \right]^{1/2}
  \]

  Note: The peak electric field decreases in forward bias. Reverse bias increases the field strength.

- Note: potential step and depletion region changes are the same as happens in a p-n junction.
Applying bias to a metal-semiconductor junction, cont.

- **Currents**
  
  Note: the barrier seen by electrons in the metal does not change with bias, whereas the barrier seen by those in the semiconductor does.

  Thus the carrier flux (current) we focus on is that of majority carriers from the semiconductor flowing into the metal. Metal-semiconductor junctions are primarily majority carrier devices.

  Minority carrier injection into the semiconductor can usually be neglected; more about this later
Applying bias to a metal-semiconductor junction, cont.

• Currents, cont.

The net current is the current from the semiconductor to the metal, minus the current from the metal to the semiconductor:

\[ i_D(v_{AB}) = i_{Dm\rightarrow s}(v_{AB}) - i_{Ds\rightarrow m}(v_{AB}) \]

**Semiconductor to metal, \( i_{Ds\rightarrow m}(v_{AB}) \)**

Four factors:
1. \( A \), the cross-sectional area
2. \(-q\), the charge per carrier
3. \( N_{D_n} \exp\left[-q(\phi_b - v_{AB})/kT\right] \), the number of carriers that can cross the barrier, \( (\phi_b - v_{AB}) \)
4. \( R \), the velocity at which those carriers cross the junction region

\[ i_{Ds\rightarrow m}(v_{AB}) = -q \ A \ R \ N_{D_n} \exp\left[-q(\phi_b - v_{AB})/kT\right] \]

**Metal to semiconductor, \( i_{Dm\rightarrow s}(v_{AB}) \)**

Not a function of voltage (because barrier seen from metal doesn't change)

Must equal \( i_{Ds\rightarrow m}(v_{AB}) \) when \( v_{AB} = 0 \), i.e. \( i_{Ds\rightarrow m}(0) \)

\[ i_{Dm\rightarrow s}(v_{AB}) = i_{Ds\rightarrow m}(0) = -q \ A \ R \ N_{D_n} \exp\left[-q\phi_b/kT\right] \]
Applying bias to a metal-semiconductor junction, cont.

• Currents, cont.

Thus, the net current is:

\[ i_D(v_{AB}) = q A R N_{Dn} \exp(-q\phi_b/kT) [\exp(qv_{AB}/kT) - 1] \]

What we haven't done yet is say anything about \( R \) (at least not enough)
The modeling meat is in \( R \), the rate [cm/s]!

• Barrier transit rate models (models for \( R \))

Different models assume that different factors are limiting the flow, and they result in different dependences of \( R \) (and thus of the \( i_D \)) on the device and material parameters and temperature.

Thermionic emission theory - the flow is limited by the rate at which carriers try to cross the barrier

Drift-diffusion theory - the flux is limited by the rate at which carriers cross the depletion region and reach the barrier

Combination theories - both of the above factors play a role and must be included in the modeling
Applying bias to a metal-semiconductor junction, cont.

• Image force barrier lowering

An electron leaving a metal sees an image force pulling it back:

\[ \phi(x) = \frac{q^2}{16\pi d^2} \]

We see that the potential step at the surface of a metal is not abrupt as we have modeled it:

\[ q\phi_m \]

This reduces the barrier seen by the carriers.

(next foil)
Applying bias to a metal-semiconductor junction, cont.

• Image force barrier lowering (cont.)

The image force reduces the barrier when an electric field $E_x$ is applied normal to surface:

In the case of a M-S junction:

\[ E_x(\approx 0) = \frac{qN_D x_D}{\varepsilon_s} = \sqrt{\frac{2\varepsilon_s N_D (\phi_b - \nu_{AB})}{q}} \]

The barrier reduction increases with increasing reverse bias (increasing $|E_x|$) and is larger when the doping level is higher.

This means the current does not saturate in reverse bias (unlike a p-n diode), and is larger on a heavily doped specimen.
Comparison of m-s junctions and p-n junctions

Lessons from i-v modeling results:
– Comparing metal to n-Si and p⁺-Si to n-Si diodes, i.e. same n-sides

• The m-s current is higher at the same bias (m-s barrier is always lower)
  \[ i_{D,m-s}(v_{AB}) > i_{D,p-n}(v_{AB}) \text{ at same } v_{AB} \]

• There is no minority carrier injection or storage in the m-s diode
  modulation and switching can be much faster

• The reverse bias, or "off" current of an m-s diode does not truly saturate
  turn-off is not hard, but we can still have sharp breakdown and avalanche

The first two differences play major roles in several applications of m-s diodes
What metal-semiconductor junctions are good for

Note: The key features that make m-s junctions useful are...
- majority carrier devices, negligible minority carrier injection
- relatively low barrier to forward current flow
- depletion and field extend to surface

Important Applications

• Ohmic contacts
  an essential component of any electronic device

• Determining doping profiles
  a key diagnostic technique in device fabrication/processing

• Shunt diodes
  to reduce switching transients in bipolar transistor logic

• Microwave diodes
  another use taking advantage of negligible excess carrier injection

• FET gate (MESFETs)
  the subject of Lecture 7

• Ultraviolet detectors
  to be discussed in Lecture 22