Lecture 8 - Heterojunction FETs - General HJFETs, HFETs

• General principles of heterostructure use in FETs
  Specific applications
  Improving substrate isolation
  Improving gate characteristics
  Improving channel conductance

• HFETs - doped channel HJFETs
  Basic structure
  Device enhancement using pseudomorphic layers
    Strained channels
    Strained gate
  Undoped channel HJFETs
    Basic structure
    Complementary HIGFET logic

• HEMTs, MODFETs, TEGFET, MISHFET, MOSHFET
  Basic structure
  Devices based on GaAs, InP, GaN
  Charge control analysis
  Nitride HEMTs and polarization doping

• Compound Semiconductor Magazine - free at: http://compoundsemiconductor.net/subscribe/CS/code7
Heterojunction FETs - improving the MESFETs with heterojunctions

**Gate characteristics:**
- barrier height
- leakage current

**Channel conductivity:**
- carrier concentration
- carrier mobility

**Substrate isolation:**
- reducing injection

There are improvements we can make in all of these areas
**Improving substrate isolation** - lower boundary of the MESFET channel is not abrupt

**A. Channel-substrate interface**

**B. Lower confinement**

- Carriers can "spill out" of the channel into the substrate
  - the gate then has less control ($g_m$ suffers)
  - these carriers don't respond to the signal on the gate (response time suffers)
  - output characteristics don't saturate well ($g_o$ is large)

Quite gradual if on undoped SI substrate
Spill out into substrate
- a Monte Carlo simulation

A. Spatial distribution
   at one instant

B. Equipotential lines

• What are some solutions?
  - wide bandgap buffer layer
  - p-type substrates
  - low temperature, high arsenic content buffer
  - air isolation
  - polarization
Solutions for substrate isolation - wide bandgap buffer layer

- Undoped AlGaAs buffer layer
  - Lower barrier for confinement
  - Confining barrier ($\Delta E_c \approx 0.8x \text{ eV}$)

- This type of wide bandgap buffer is widely used, but this barrier is not infinite and once in the AlGaAs the carriers can move into the substrate.
Solutions for substrate isolation - low temperature, high arsenic content buffer

GaAs grown by MBE at $\approx 200^\circ C$ with excess As:
1) is semi-insulating
2) has a large mid-gap state density
3) has a very short carrier lifetime

With a large electronic state density in the buffer the depletion region is very narrow.

• Now the barrier may be even higher and the carriers that surmount it have a very short lifetime. Note: The use of Cr- or Fe-doped SI substrates has a similar effect but these have proven difficult to reproduce and control in GaAs.
Solutions for substrate isolation - air isolation

The availability of selective wet etches makes it possible to use an air buffer:
1) AlAs spacer grown during epitaxy
2) mesa etched through AlAs layer and leads patterned to the substrate
3) selective etch (HF or HCl) used to remove AlAs

- Primarily a research novelty in the FET world, but we will see this idea used to create air gaps for use in other devices later on.
- Thermal management is difficult
Improving gate characteristics - limited by low Schottky barrier height

We would really like to have an insulated gate as in a MOSFET, but surface states have precluded realization of stable, hysteresis-free MIS capacitors on the III-Vs. (The closest people have come is to achieve very limited success sulfidizing GaAs and to depositing SiO₂ on InP.)

A wide bandgap semiconductor can be used as a pseudo-insulator to get something approaching MOS action.

A wide bandgap gate "dielectric" can have two benefits:
- increase barrier effectiveness, thereby increasing the degree to which the channel can be turned on.
- place the gate closer to the channel carriers (because the barrier is thin and because it has a high dielectric constant) thereby increasing its control over them, i.e., increasing $g_m$. 
Solutions for the gate - wide bandgap "dielectric"

The structure:

A good rule of thumb with Al$_x$Ga$_{1-x}$As-GaAs HJs is that $\Delta E_c \approx 0.8 \Delta E_g$ eV)

With gate bias:

- With forward bias on the gate the channel charge can actually be increased above the background doping with accumulation occurring at the hetero-interface.
Improving channel conductance - \( g_m \) and \( \omega_t \) both improve with higher channel conductance

To get higher channel conductance one must...
- use higher mobility materials (channel vs access regions), and/or
- get more carriers into the channel

To do this:
- Increase the barriers (top and bottom) to get more carriers into the channel (we just saw this)
- Use \( \text{In}_x\text{Ga}_{1-x}\text{As} \) to increase the electron mobility (we talked about pseudomorphic and metamorphic layers earlier)
- Use modulation doping
  (An important cause of scattering is ionized impurities, and higher doping levels result in lower mobilities, so the conductivity goes up only slightly. Device noise also increased significantly. A solution is modulation doping.)
Modulation doping - separating dopants and carriers

Demonstration structure:

- The objective is to increase the carrier mobility and reduce the noise associated with ionized impurity scattering.
Modulation doping - separating dopants and carriers

Mobility comparison:

- Carrier mobility is increased and scattering noise is reduced.
The HFET zoo...

- Doped channel HJFET
- Undoped HJFET
- HIGFET
- JFET
- HEMT, MODFET, TEGFET, SDFET
- mmHEMT
- pHEMT
- PolFET
- MOSHFET
- MISHFET
- CAVET
- ...
**Heterojunction FETs - the doped channel HJFET (the HFET)**

**Structure:**
- a wide bandgap layer under the gate
Doped channel HJFET - the HFET

**Pseudomorphic InGaAs and InAlAs on InP**: strained layers

- The carrier mobility can be increased and the barrier height can be raised if strained layers are used. Both were studied....

- We will look at the results obtained for both approach in turn.

  Work of Prof. Jesus del Alamo and his students at MIT.
Doped channel HJFET - the HFET

Pseudomorphic InAlAs barriers: increasing barrier height

Doped channel HJFET - the HFET

Pseudomorphic InGaAs channels:
increasing channel mobility
and barrier height

Ref: S. Bahl and J. del Alamo, 2nd Int. Conf. On
InP and Related Compounds, unpublished.
Heterojunction FETs - the undoped HJFET
(the HIGFET - heterojunction insulating gate FET)

**Structure:**
- undoped hetero-structure
- the HFET analog of the inverted channel MOSFET

Unbiased bands under the gate:

Carriers are drawn into the channel by the gate and from the doped regions. They can be either holes or electrons.
**Undoped HJFET - the HIGFET**

**Complementary devices:** the same epi-structure can be used to make n-channel and/or p-channel HIGFETs

- We can make both n- and p-channel FETs from the same epi-structure.

- **Issues:**
  - p-channel device still suffer from low hole mobility
  - sources and drain resistances are a major concern
  - can only be enhancement mode

Developed at Honeywell
Complementary HIGFET Logic - HFET CMOS

Inverter with n- and p-channel enhancement mode HIGFETs

\[
\begin{align*}
&+1 \text{ V} \\
&V_p = 0.5 \text{ V} \\
&-V_p = -0.5 \text{ V} \\
&v_{IN} \\
&v_{OUT} \\
&\text{Grd.}
\end{align*}
\]

<table>
<thead>
<tr>
<th>$v_{IN}$</th>
<th>n-channel</th>
<th>p-channel</th>
<th>$v_{OUT}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 V (lo)</td>
<td>Off</td>
<td>On</td>
<td>1 V (hi)</td>
</tr>
<tr>
<td>1 V (hi)</td>
<td>On</td>
<td>Off</td>
<td>0 V (lo)</td>
</tr>
</tbody>
</table>

Just as with CMOS, the attraction is that static power is eliminated because one device is always off in steady-state.
Heterojunction FETs - JFET

Structure:
- JFETs can be viewed as improved MESFETs with an oppositely doped layer having been inserted under the gate; it might even be wider bandgap

The gate performance is much improved:
- lower leakage
- larger forward turn-on voltage

Comments on JFETs:
- can be made both n- and p-channel
- gate lengths can be made as those of MESFETs
- requires making ohmic contacts to both n- and p-type
- only being pursued in small, low level efforts at several companies
Heterojunction FETs - the HEMT; also called MODFET, TEGFET, and SDFET)

Structure:
- doped WBG layer over an undoped NBG layer

Typical doping level in AlGaAs: \(10^{18} \text{ cm}^{-3}\)
Typical sheet carrier density in channel: \(10^{12} \text{ cm}^{-2}\)
(\(3 \times 10^{13} \text{ cm}^{-2}\) in AlGaN/GaN)
Modulation doped HJFETs - the HEMT

The most important problems associated with the HEMT deal with the n-doped AlGaAs gate

To understand this, consider turning the channel on:
- The maximum forward bias that can be applied to the gate is set by the onset of conduction in the AlGaAs

Moderate forward bias:
  n-AlGaAs depleted

Excessive forward bias:
  n-AlGaAs populated, parallel conduction and gate leakage
HEMTs - Delta Doping
The parallel conduction problem can be reduced by not doping the entire AlGaAs, but instead to put the dopants in a single layer:

- Delta doping yields higher channel concentrations
HEMTs - Delta Doping, cont.

An example of a device with a delta-doped AlGaAs barrier above, as well below, the channel:

2.5 x 10^{12} \text{ cm}^{-2}

2.5 x 10^{12} \text{ cm}^{-2}

4 x 10^{12} \text{ cm}^{-2}

Work of T. Kuo et al at MIT and AT&T Bell Labs
HEMTs - the DX Center problem

Solving the problem of AlGaAs turn-on:
- The obvious solution is to increase the Al concentration to increase this layer's bandgap.
- The problem is the appearance of DX centers above \( \approx 23\% \) Al.

**DX Center:** A deep level associated with the L-band minimum

HEMTs - the DX Center problem, cont.

Why DX centers are a problem:
They cause problems at low temperatures:
- I-V collapse
- persistent photoconductivity

I-V collapse:

Al fraction must be less than 20%
(barrier ≈ 0.16 eV)

The solution: Don't make the barrier higher, make the well deeper by adding indium. This involves strained layers....

Pseudomorphic HEMTs (PHEMTs)
**HEMTs - the pseudomorphic HEMT (PHEMT)**

The problem of DX centers with high Al fraction layers led to the development of the pseudomorphic HEMT, or PHEMT:

![Diagram](image)

- Undoped AlGaAs spacer
- Strained undoped InGaAs channel (≈15% In)
- 0.4 eV

This structure was first developed at the University of Illinois.
HEMTs - the InGaAs/InAlAs HEMT on InP

Another solution to the problem of DX centers in high Al fraction AlGaAs layers is to use the InGaAlAs system on InP:

- 0.5 eV barriers
- no DX centers in InAlAs
- mobility and saturation velocity 50% higher than in GaAs

This has proven to be a very successful structure: very low noise and very fast. Used extensively in satellite receivers.
HEMTs - the Metamorphic HEMT (mmHEMT) on GaAs

A recent DX center solution that doesn't require expensive InP substrates is the metamorphic HEMT:

- we talked earlier about step and linear grading of such buffers
- the next question is: How high an In composition is optimal?

3" InP: $700
4" GaAs: $170

Relaxed device epilayers
InGaAs graded buffer (relaxed)
mmHEMTs - what In fraction?

There is a trade-off between low field mobility and sheet carrier concentration in the channel:

- Conduction band barrier
- Mobility vs. Sheet density

- the presently accepted "optimum" seems to be about 30% In

There is no general agreement on which approach is superior and the choice often one of convenience and/or practicality and/or IP.

Because the last layer is often not fully relaxed, it is common to grade to a certain level and then step back, as seen in the structure on the left. In this way a fully relaxed top structure can be realized.
InAs 5 nm

<table>
<thead>
<tr>
<th></th>
<th>In$<em>{0.65}$Ga$</em>{0.35}$As</th>
<th>In$<em>{0.53}$Ga$</em>{0.47}$As</th>
<th>In$<em>{0.52}$Al$</em>{0.48}$As</th>
</tr>
</thead>
<tbody>
<tr>
<td>n+ Cap</td>
<td>5 nm</td>
<td>15 nm</td>
<td>15 nm</td>
</tr>
<tr>
<td>Stopper</td>
<td>InP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Barrier</td>
<td>In$<em>{0.52}$Al$</em>{0.48}$As</td>
<td>8 nm</td>
<td></td>
</tr>
<tr>
<td>5-doping</td>
<td>Si (5 x 10$^{12}$/cm$^2$)</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Spacer</td>
<td>In$<em>{0.52}$Al$</em>{0.48}$As</td>
<td>3 nm</td>
<td></td>
</tr>
<tr>
<td>Channel</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>2 nm</td>
<td>InAs</td>
</tr>
<tr>
<td></td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>5 nm</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
</tr>
<tr>
<td>Buffer</td>
<td>In$<em>{0.52}$Al$</em>{0.48}$As</td>
<td>500 nm</td>
<td></td>
</tr>
</tbody>
</table>

3 Inch S. I. InP Substrate
Charge control analysis in HEMTs

\[ n_s (V_G) \]?
Quantum capacitance?
Charge sharing?
Pinch-off voltage?
Modulation efficiency?
Charge control model for the MODFET... $n_s(V_{GS})$

![Diagram of charge control model for the MODFET](image)

Mishra and Singh (2008)
The Role of Inefficient Charge Modulation in Limiting the Current-Gain Cutoff Frequency of the MODFET

MARK C. FOISY, STUDENT MEMBER, IEEE, PAUL J. TASKER, BRIAN HUGHES, ASSOCIATE MEMBER, IEEE, AND LESTER F. EASTMAN, FELLOW, IEEE

Fig. 2. Variation of \( n_{2D} \) and the free and bound components of \( n_{SL} \) with gate-to-channel voltage for a conventional MODFET. The dotted line shows the non-saturating sheet density \( n_{2D}^* \) that would exist in the absence of parasitic supply layer charge.

Fig. 3. \( f_t \) versus \( I_D \) for 1-\( \mu \)m conventional (dashed line) and pseudomorphic (solid line) MODFETs including the effect of fringe and pad capacitances.

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Lecture 8 - Slide 36
POLARIZATION DOPING
and
AlGaN/GaN HEMTs
Figure 8.18: (a) Stick-ball representation of Wurtzite GaN crystal structure. (b) Classical model of polarization charge in a polar material such as GaN. (c) Crystal will draw in charge to screen the polarization dipole - From M. J. Murphy et al, MRS Internet J. Nitride Semicond. Res. 4S1, G8.4(1999)
Spontaneous polarization and piezoelectric constants of III-V nitrides

Fabio Bernardini and Vincenzo Fiorentini
INFM, Dipartimento di Scienze Fisiche, Università di Cagliari, I-09124 Cagliari, Italy

David Vanderbilt
Department of Physics and Astronomy, Rutgers University, Piscataway, New Jersey 08845-0849
(Received 9 May 1997)

TABLE II. Calculated spontaneous polarization (in units of C/m\(^2\)), Born effective charges (in units of e), and piezoelectric constants (in units of C/m\(^2\)) for III-V wurtzite nitrides and II-VI wurtzite oxides. Theoretical results for ZnO and BeO are included.

<table>
<thead>
<tr>
<th></th>
<th>(P^{eq})</th>
<th>(Z^*)</th>
<th>(d\mu/d\varepsilon_3)</th>
<th>(\epsilon_{33})</th>
<th>(\epsilon_{31})</th>
<th>(\epsilon_{33}^{(0)})</th>
<th>(\epsilon_{31}^{(0)})</th>
</tr>
</thead>
<tbody>
<tr>
<td>AlN</td>
<td>-0.081</td>
<td>-2.70</td>
<td>-0.18</td>
<td>1.46</td>
<td>-0.60</td>
<td>-0.47</td>
<td>0.36</td>
</tr>
<tr>
<td>GaN</td>
<td>-0.029</td>
<td>-2.72</td>
<td>-0.16</td>
<td>0.73</td>
<td>-0.49</td>
<td>-0.84</td>
<td>0.45</td>
</tr>
<tr>
<td>InN</td>
<td>-0.032</td>
<td>-3.02</td>
<td>-0.20</td>
<td>0.97</td>
<td>-0.57</td>
<td>-0.88</td>
<td>0.45</td>
</tr>
<tr>
<td>ZnO</td>
<td>-0.057</td>
<td>-2.11</td>
<td>-0.21</td>
<td>0.89</td>
<td>-0.51</td>
<td>-0.66</td>
<td>0.38</td>
</tr>
<tr>
<td>BeO</td>
<td>-0.045</td>
<td>-1.85</td>
<td>-0.06</td>
<td>0.02</td>
<td>-0.02</td>
<td>-0.60</td>
<td>0.35</td>
</tr>
<tr>
<td>ZnO(^a)</td>
<td>-0.05</td>
<td>-2.05</td>
<td>-0.25</td>
<td>1.21</td>
<td>-0.51</td>
<td>-0.58</td>
<td>0.37</td>
</tr>
<tr>
<td>BeO(^a)</td>
<td>-0.05</td>
<td>-1.72</td>
<td>-0.09</td>
<td>0.50</td>
<td>—</td>
<td>-0.29</td>
<td>—</td>
</tr>
</tbody>
</table>
AlGaN/GaN HEMTs: Polarization

In a HEMT:

Polarization discontinuities @ interfaces → fixed charge densities → build-in electric fields → 2DEG

But Polarization can be more useful than only that…
Mishra and Singh, Springer.

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Fig. 12. The dependence of $n_s(x)$ on the barrier thickness calculated using equation (50) for $x = 0.15$, 0.30, and 0.45 are shown. A drastic decrease in sheet carrier concentration is predicted for thicknesses below 12, 8, and 6 nm, respectively. For $x = 0.3$ the sheet carrier concentration of AlGaN/GaN heterostructures was measured by CV-profiling for barrier thicknesses between 1 and 50 nm. These data (white open symbols) and experimental results of other groups (black and grey symbols [53, 55]) are in good agreement with the theoretical predictions.

phys. stat. sol. (c) 0, No. 6, 1878–1907 (2003) / DOI 10.1002/pssc.200303138
Ultra-thin InGaN layers to increase the electron confinement in GaN HEMTs

In a GaN-ultrathin InGaN-GaN structure, the polarization-based electric field in the InGaN layer induces a discontinuity (downwards) in the conduction band…

\[ \Delta E_c \]

\[ \Delta E_p = 0.17 \text{ eV in 10 Å of 10\% InGaN} \]

\[ 0.32 \text{ eV in 10 Å of 20\% InGaN} \]

When we apply this idea to an AlGaN/GaN HEMT…

Conduction band similar to a double heterojunction structure

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T. Palacios et al., Electron Dev. Letts. Vol. 27, 13
Std. HEMT vs InGaN back-barrier: *Improvement in the pinch-off*

InGaN back-barrier → Better 2DEG confinement → Excellent pinch-off

*even at $V_{DS} > 50 \text{ V}$ and $L_G < 200 \text{ nm}$*
Figure 8.19: Schematic diagram of an n-type GaN sample along with charge profile and band diagram (a) during the initial stages of growth, (b) for $d = d_{cr}$, and (c) for $d > d_{cr}$.

Mishra and Singh, Springer.
Figure 8.20: Schematic diagram of an $n$-type GaN sample along with charge profile and band diagram when the effects of surface states are taken into account. (a) Very thin GaN, for which surface states are not ionized. (b) Once GaN is thick enough such that $E_{DD}$ is very close to $E_F$ at the GaN surface, surface donors become ionized and polarization charge is screened.

Mishra and Singh, Springer.

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