WIN has joined a select band of chip makers with its own BiFET technology. The H2W foundry process optimizes HBTs and PHEMTs independently, and it integrates power amplifiers, low-noise amplifiers, logic control and a power switch on a single chip, says Cheng-Kuo Lin.

Ruthless component price erosion is prevalent in the highly competitive market of front-end modules (FEMs) for cellular phones. To stay competitive, chip makers have to reduce their manufacturing costs by reducing die size and count, and increasing functionality, which ultimately lowers overall component costs. At the same time, the FEM's performance has to undergo continual improvement to satisfy the desires of handset system designers.

GaAs still offers an RF performance advantage over silicon technologies, such as SiGe and BiCMOS, but it is falling behind in terms of cost and the level of integration. To address this weakness, most component manufacturers in the RF industry integrate several technologies into a multichip module (MCM) package, such as the HBT-based power amplifier (PA), PHEMT switch, CMOS controller and surface-mount passives. However, this approach suffers from high packaging costs that typically account for half of the overall bill of materials.

Recently, GaAs chip makers – including the US manufacturers Anadigics, Skyworks and TriQuint – have addressed this weakness by monolithic integration of the HBT and E/D-PHEMT. These sophisticated chips, which are often referred to as BiFETs, can eliminate the cost associated with MCM packaging. Now foundry customers can get access to this technology and receive an additional benefit – simplification of supply-chain management.
At WIN Semiconductors, a GaAs foundry based in Taoyuan, Taiwan, we are now offering our version of BiFET technology that we call H²W. This 150 mm GaAs process, which we released earlier this year, integrates the InGaP HBT, E/D-mode PHEMTs and various passive components, including backside through via holes (see box "WIN Semiconductors’ H²W process").

Our H²W process enables a HBT-based PA, a D-mode PHEMT switch, an E-mode PHEMT low-noise amplifier and an E/D-mode PHEMT logic control circuit to be combined on a single GaAs chip, free from external passive elements. Circuit designers can access the HBT and PHEMT technologies simultaneously and take the best advantages of each device type without any compromise in performance.

Our H²W technology provides great design flexibility and novel circuit opportunities. For example, a PHEMT switch can be configured to produce a bypass circuit that boosts the efficiency at low power in a multiple-stage HBT (figure 1). Alternatively, the HBT's base-collector diode can act as the electrostatic damage (ESD) protection diode for PHEMT switches. This can address the issue of an unacceptably large real estate occupied by the Schottky ESD protection diode, which is a key drawback of the stand-alone PHEMT process. Other possible PA circuit designs that can benefit from the H²W process include a bias control switch, a power control circuit and a current limiter. These opportunities are just a few examples. We believe that many other high-performance circuit designs are possible once engineers gain more experience with our mixed device technology.

The epiwafers for our H²W process are grown by MOCVD on semi-insulating GaAs and feature a stacked layer structure with the InGaP HBT on top of the PHEMT. Such a design is suitable for high-volume, low-cost manufacturing because it uses the single growth approach and avoids the selective regrowth technique pioneered by TRW in the 1990s.

The H²W process eliminates additional parasitic capacitance in the PHEMT by placing the HBT on top of this device. With this geometry the undoped InGaP etch-stop layer isolates any influence that the PHEMT has on HBT performance. Skyworks, in comparison, adopts a different approach. The emitter layer is used as the channel layer for FET fabrication. In this
case, parasitic capacitance could affect the FET's RF performance, but that is not a major concern because this transistor's function is primarily to improve the bias circuit.

The other strength of our technology is the use of an InGaP etch-stop layer that fully separates the HBT and PHEMT. With our H\textsuperscript{2}W process, the HBT and PHEMT do not share any epitaxial layers, which means that it is possible to optimize the HBT and the E/D-mode PHEMT separately. This is different from Skyworks' and Anadigics' designs. Skyworks uses the HBT's emitter layer as the channel for its FET, while Anadigics shares its thick, highly doped collector layer between both transistors.

Our HBT's structure is ideal for cellular handset applications because it combines a high-power output with a rugged design. The PHEMT benefits from an epitaxial structure that is compatible with a double selective gate recess etch process, which means that the AlGaAs and InGaAs layers can be used for the Schottky barrier and the channel, respectively. We have also selected the layer thicknesses, doping concentration and composition of the III-V alloys to optimize the trade-off between characteristics such as breakdown voltage, on-resistance, pinch-off voltage, transconductance and gate lag.

These H\textsuperscript{2}W processing steps form HBTs and PHEMTs separated by 25 µm that are clearly visible in cross-sectional scanning electron microscopy images (figure 2). The wide recesses of the devices illustrate that it is possible to develop a process that can reliably control the gate's dimensions.

Our H\textsuperscript{2}W process can reliably yield high-quality PHEMTs and HBTs on the same chip (table 1). Both D and E-mode PHEMTs, for example, deliver a drain current from a 100 ns pulse that is greater than 90% of the value from continuous operation. This indicates that they are suitable for serving applications requiring high frequencies and power densities combined with a fast switching time for PAs and switches.
Tests on our 2 × 75 µm E-mode PHEMT operating at 3.5 GHz, which is biased at a source-drain voltage of 5 V and produces a source-drain current of 130 mA/mm, reveal a maximum power-added efficiency (PAE) of 64.3% and an output power of 392 mW/mm. Meanwhile, our 8 × 25 µm E-mode PHEMT produced a minimum noise figure of 0.44 dB at 3 GHz and 16.7 dB of gain, under the conditions of 3 V and 75 mA/mm.

![Figure 3](image)

We have also investigated the performance of single-pole, double-throw switches fabricated with our H²W multigate process technology (figure 3). At 900 MHz, they produce a 0.45 dB insertion loss (the difference between the signal at the transmitter and the antennae) and more than 25 dB of isolation (the ratio of the signal at the transmitter and receiver).

Harmonic testing has been carried out to assess this switch's linearity and has proved that our H²W optical gate lithography process is suitable for multiple-gate high-power and high-linearity applications using low control voltages.

![Figure 4](image)

We have also assessed our InGaP HBT's performance. These transistors have a typical turn-on voltage of 1.26 V and feature a base layer designed to deliver a DC current gain of 78. PAs built with these devices and operating at 900 MHz produced 34.5 dBm at 63% PAE (figure 4). Tests to assess the ruggedness of this amplifier, which revealed a voltage-standing-wave ratio of 12 for all input phases under the conditions of a collector-emitter voltage of 3.6 V and an input power of 27 dBm, demonstrate that this device is robust without sacrificing power.

Reliability tests have been performed on both types of transistor. The D- and E-mode PHEMTs pass our internal 500 h test at 165 °C, using source-drain voltages and currents of 8 V and 80 mA/mm, respectively. Meanwhile, the HBTs show no decline in current gain after operating for 1000 h at an ambient temperature of 125 °C.

This series of tests demonstrates the reliability and performance of HBTs and PHEMTs united by the H²W process. In addition, it shows that fabless designers of PAs now have access to a foundry process that can produce highly integrated RF transceivers and novel RFIC circuits. The
H$_2$W approach may still be in its infancy in terms of circuit design but it will now have an increasingly important role to play in the evolution of handset FEMs.

**About the author**

Cheng-Kuo Lin is the project manager of WIN's HEMT product technology development division. He joined the company in 2004 after completing a PhD at National Central University, Taiwan.