SILICON CARBIDE POWER DEVICES

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Outline:

- Why Silicon Carbide?
- Applications
- Schottky Diodes
- MOSFETS
- Challenges
- Conclusion
Material Properties:

- Wide Bandgap, $E_G = 3.26$ ev for 4-H SiC
  - Lower leakage currents in PN junction
  - Large barrier height $\rightarrow$ Low leakage in Schottky

- $n_i = \sqrt{N_C N_V} e^{-(E_G/2KT)}$
  - Lower $n_i$ at high $T$ $\rightarrow$ suitable for high $T$ applications

- Reduced impact ionization coefficients at given electric field
  - High Breakdown Voltages

- Lower drift region resistance
  - $R_{on,sp} = \frac{W_D}{q\mu_n N_D} = \frac{4(BV)^2}{\varepsilon_s \mu_n E_C^3}$
    - $E_C$ higher in SiC $\rightarrow$ $R_{on,sp}$ lower

- High Thermal Conductivity
Applications:

- SiC heavily used in high-end Power Factor Correction Systems (PFC)
- Schottky Barrier Diodes commercially available up to 1200V/50A
Schottky Rectifiers:

\[ R_{\text{drift}} = \frac{W_D}{q\mu_n N_D} = \frac{4(BV)^2}{\varepsilon_s \mu_n E_C^3} \]

\( E_C \) higher in SiC \( \rightarrow \) \( R_{\text{drift}} \) lower

On-state voltage drop,

\[ V_F = \frac{kT}{q} \ln\left(\frac{J_F}{J_S}\right) + J_F (R_{\text{drift}} + R_{\text{sub}}) \]

\[ J_S = AT^2 \exp\left(\frac{-q\phi_b}{kT}\right) \]

\( V_F \downarrow \) when \( R_{\text{drift}} \downarrow \)

Leakage Current increases at high electric field due to

(a) barrier lowering \( \Delta \phi_b = \sqrt{\frac{qE_m}{4\pi\varepsilon_s}} \)

(b) Field-assisted tunneling

\( E_m \) is high in SiC \( \rightarrow \) Large reverse leakage currents

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Junction Barrier Schottky Rectifiers (JBS):

Potential Barrier of P-N junction shields the schottky contact from high fields

- Voltage drop across diode not enough to forward bias PN junction
- P+ region formed by ion-implantation
- $\Delta \phi_b \downarrow$ due to lower field at schottky
  - lower leakage current
- $d \downarrow \rightarrow R_{on} \uparrow$ due to current crowding
- $d \uparrow \rightarrow E_{schottky} \uparrow$
Trench Schottky Barrier Schottky Rectifiers (TSBS):

Potential Barrier for shielding contact from high fields created by MS junctions:

- Second metal has larger barrier height
- Ni often used as HB metal as Ti for LB
- On-state current flows through LB contact
  - $\Delta \phi_b$ ↓ due to lower field at LB schottky
  - $\rightarrow$ lower leakage current
- Leakage current due to HB junction negligible
- Processing adv. over JBS as ion implants in SiC need very high $T$ anneals which can damage semiconductor surface
Sample Device Characteristics:

Schottky diodes up to 1200V/50A available commercially through CREE.

1200V/20A CREE device:
Forward voltage drop of 2V
Reverse Current of 10 $\mu$A
Challenges:

- Reverse leakage currents can be significantly higher in presence of defects because of localized barrier lowering
  → Need defect free samples
- High T annealing of implants can damage SiC surface
- Rough semiconductor surfaces increase leakage currents
- Surface damage can be minimized using carbon cap during annealing
- E-field crowding at edge of schottky metal contacts
  - guard rings, field plates, Argon implants to produce high R regions
- Cost of SiC diodes still much higher than Si alternatives
  4-inch wafers in CREE in 2007
Trench MOSFET (U-MOSFET):

Parasitic bipolar suppressed by shorting N+ source and P-Base

Large leakage if p-Base completely depleted
Careful design to prevent BV limiting

\[ R_{on} = R_{CH} + R_D + R_{sub} \quad R_{CH} \alpha \frac{1}{\mu_n} \]

Low inversion layer mobility could make \( R_{CH} \) dominate \( R_D \)

High \( V_T \) due to high doping in base to prevent punch through

Electric field in oxide=3X field in drift region
High Electric fields at gate ox interface \( \rightarrow \) reduced breakdown voltages

[1]
Planar MOSFET (D-MOSFET):

Parasitic bipolar suppressed by shorting N+ source and P-Base

Large leakage if p-Base completely depleted
Careful design to prevent BV limiting

\[ R_{on} = R_{CH} + R_A + R_{JFET} + R_D + R_{sub} \]

\[ R_{CH} \propto \frac{1}{\mu_n} \]

\( R_{on} \) higher than in Trench MOSFET
Low inversion \( \mu \rightarrow R_{CH} \) dominate \( R_D \)

High \( V_T \) due to high doping in base to prevent punch through

BV slightly higher due to elimination of oxide corner at peak field
Shielded Planar MOSFET:

P+ region shields gate oxide from high fields → Higher breakdown voltages

P+ region eliminates punch-thru of P-base → Lower channel length → Lower doping in base → lower $V_T$

Can design as accumulation mode with N-Base Acc. Mode mobility is higher → Lower $R_{on}$
Sample Device Characteristics:

CREE 1200V, 10A SiC DMOSFET

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Boost Converter Efficiency
Cooling fan disabled at t=0
Challenges:

- SiC switches still far from being commercially available
- Low channel mobilities due to high SiC/SiO$_2$ interface state densities
- Interface states also increase leakage due to trap-assisted tunneling
- Most research on improving quality and reliability of gate oxides
  - Deposited oxides using CVD, sputtering or MBE
  - Partial oxidation of silicon layer deposited on SiC substrate
  - Alternative dielectric materials such as HfO$_2$ and Al$_2$O$_3$
Conclusions:

- The wide bandgap and high thermal conductivity of SiC make it an ideal candidate for high voltage and high temperature applications
- SiC Schottky diodes up to 1200V / 50A commercially available
- Lot of interest in using SiC for switches.
  - MOSFETs are the most researched, but some work in JFETs and BJTs as well
- Main show-stopper for MOSFETs is low electron mobility and oxide reliability
References: