6.012 Electronic Devices and Circuits

Exam No. 2

Wednesday, April 6, 2011
Room 32-141
7:30 to 9:30 pm

Notes:

1. An effort has been made to make the various parts of these problems independent of each other so if you have difficulty with one item go on, and come back later.

2. Some questions ask for an explanation of your answer. No credit will be given for answers lacking this explanation.

3. Unless otherwise indicated, you should assume room temperature and that kT/q is 0.025 V = 25 mV. Also, use the 60 mV rule, i.e. approximate [(kT/q) ln 10] as 0.06 V.


5. The best way to receive partial credit is to show your work. All of your answers and any relevant work must appear on these pages. Any additional paper you hand in will not be graded.

6. Make reasonable approximations and assumptions. State and justify any such assumptions and approximations you do make.

7. Be careful to include the correct units with your answers when appropriate.

8. Be certain that you have all nine (9) pages of this exam booklet and the five (5) page formula sheet, and make certain that you write your name at the top of this page in the space provided.

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PROBLEM 1 __________  (out of a possible 20)

PROBLEM 2 __________  (out of a possible 40)

PROBLEM 3 __________  (out of a possible 40)

TOTAL
Problem 1 - (20 points)

(I) You are given a silicon MOSFET with the source, drain, and substrate terminals shorted together as shown below on the left, and you are told to measure the small signal linear equivalent gate capacitance, \(C_{gs}\), as you vary the gate bias, \(V_{GS}\), from -2.5 V to +2.5 V. You obtain the curve shown below on the right.

![Diagram of MOSFET with gate capacitance curve]

\[C_{gs} \text{ [F/cm}^2\text{]}\]

\[V_{GS} \text{ [V]}\]

\[-2.0 \quad -1.0 \quad 0 \quad 1.0 \quad 2.0\]

a) [2pts] What is the threshold voltage, \(V_T\), of this MOSFET? Indicate in the space below how you got your answer.

\[V_T = \text{Volts}\]

b) [2pts] What is the flatband voltage, \(V_{FB}\), of this MOSFET? Indicate in the space below how you got your answer.

\[V_{FB} = \text{Volts}\]

c) [2pts] Is this an n-channel or p-channel MOSFET? Explain your answer.

_____ p-channel _____ n-channel because

d) [2pts] Is this an enhancement- or depletion-mode MOSFET? Explain your answer.

_____ Enhancement-mode _____ Depletion-mode because

e) [2pts] How thick is the gate oxide, \(t_{ox}\), of this device? Indicate in the space below how you got your answer.

\[t_{ox} = \text{nm}\]
**Problem 1 continued**

(II) This part of Problem 1 concerns a well-designed n-channel MOSFET. The channel length is 0.1 µm and the mobility of the electrons in the channel is 1,000 cm²/V·s.

a) [6 pts] Consider first that the MOSFET is biased in strong inversion with $v_{GS} = V_T + 3V$, and that initially a small drain bias is applied, i.e. $v_{DS} = 0.25 V$.

i) How long does it take the average electron to travel from the source to the drain under these conditions, i.e. what is the channel transit time? Note that the MOSFET is biased in the linear region, not in saturation. Also, since $v_{DS}/2 << (v_{GS} - V_T)$ it is a good approximation to say that the channel charge density is essentially uniform under the gate and the electric field is uniform in the channel.

$$\tau_{tr} = \text{__________ s}$$

ii) Does the transit time increase, decrease, or stay the same as $v_{DS}$ is increased from 0.25V toward $(v_{GS} - V_T)$? Ignore channel length modulation. Explain your answer.

Increase _____   Decrease _____   Stay essentially the same: _____   because

iii) Does the transit time increase, decrease, or stay the same as $v_{DS}$ is increased from $(v_{GS} - V_T)$ to above $(v_{GS} - V_T)$? Ignore channel length modulation. Explain your answer.

Increase _____   Decrease _____   Stay essentially the same: _____   because

b) [4 pts] Now consider biasing the same MOSFET just below threshold at $v_{GS} = V_T - 60n mV$, and $v_{DS} = 0.25 V$.

i) What is the transit time from the source to drain in this situation? Hint: Think diode or BJT.

$$\tau_{tr} = \text{__________ s}$$

ii) How does the transit time change as $v_{DS}$ is increased upward from 0.25V? Ignore channel length modulation. Explain your answer.

Increase _____   Decrease _____   Stay essentially the same: _____   because

End of Problem 1
Problem 2 - (40 points)

(I) The circular device pictured below is fabricated in silicon with following room temperature properties: \( \mu_e = 1600 \, \text{cm}^2/\text{V-s}, \mu_h = 640 \, \text{cm}^2/\text{V-s}, \tau_{\text{min}} = 10^{-5} \, \text{s}, \) and \( n_i = 10^{10} \, \text{cm}^{-3}. \) It consists of a heavily n-doped region \( (N_D = 5 \times 10^{18} \, \text{cm}^{-3}) \) 1 \( \mu \text{m} \) deep and 5 \( \mu \text{m} \) radius, formed in a p-type substrate \( (N_A = 10^{16} \, \text{cm}^{-3}). \) The n-region is surrounded by a gate electrode with an outer radius of 15 \( \mu \text{m}. \) The gate oxide is 20 \( \text{nm} \) thick, and the electrostatic potential of the gate metal is 0.4 \( \text{V} \) relative to intrinsic Si.

![Device Diagram]

a) [4 pts] What is the flatband voltage, \( V_{\text{FB}} \), of the MOS capacitor in this device? Assume \( V_{\text{BS}} = 0. \)

\[ V_{\text{FB}} = \quad \text{V} \]

b) [4 pts] What is the threshold voltage, \( V_T \), of the MOS capacitor in this device? Assume \( V_{\text{BS}} = 0. \)

\[ V_T = \quad \text{V} \]

c) [5 pts] When \( V_{\text{GS}} = V_{\text{FB}} - 1 \, \text{V}, \) and \( V_{\text{BS}} = 0, \) what is the condition of the silicon-oxide interface under the gate, and what is the sheet charge density there?

\[ \text{_____ Accumulated    _____ Depleted    _____ Inverted, because} \]

\[ q^* = \quad \text{Coul/cm}^2 \]

d) [5 pts] When \( V_{\text{GS}} = V_T + 2 \, \text{V}, \) and \( V_{\text{BS}} = 0, \) what is the condition of the silicon-oxide interface under the gate, and what is the sheet charge density there?

\[ \text{_____ Accumulated    _____ Depleted    _____ Inverted, because} \]

\[ q^* = \quad \text{Coul/cm}^2 \]

Problem 2 continues on the next page
Problem 2 continued

e) [4 pts] With $v_{GS} = 0$, what is $n(0)$, the mobile electron density at the silicon-oxide interface under the gate, when the gate is biased so that the electrostatic potential at the interface, $\phi(0)$, is $|\phi_p| - 60 \text{ mV}$?

$$n(0) = \rule{2in}{0.1pt} \text{cm}^{-3}$$

(II) A small negative bias, $v_{BS} = -0.2 \text{ V}$, is applied to the substrate-to-source diode, and the current $i_B$ is monitored as $v_{GS}$ is varied from $V_{FB}$ to in excess of $V_T$. It is observed that $|i_B|$ is constant until the silicon-oxide interface under the gate becomes inverted, at which point it increases to a new value. This happens because when an inversion layer is induced under the gate, the area of the diode is effectively increased by that of the inversion layer. The next three questions look at this situation.

f) [4 pts] What is the substrate current, $i_B$, if $v_{GS} = V_{FB}$? Model the diode as an asymmetric $n^+\text{-}p$ diode, and assume that the current is dominated by one type of carrier, i.e. holes or electrons, as appropriate. Also, only consider the current flowing vertically across the junction (i.e. neglect current across the vertical edges of the diode), and assume short-base diode conditions apply. Neglect the depletion region widths. Finally, you may say $(e^{qV_{BS}/kT} - 1) \approx -1$.

$$i_B(\text{v}_{\text{GS}} = \text{V}_{FB}) = \rule{2in}{0.1pt} \text{A}$$

g) [4 pts] What is the substrate current, $i_B$, if $v_{GS} >> V_T$ and there is an inversion layer under the gate electrode? You may model the inversion layer-to-substrate "diode" as an asymmetrical $n^+\text{-}p$ diode identical to the $n^+\text{-}p$ diode in Part f. (Assume the current is so small that you may neglect any lateral voltage drop in the channel.)

$$i_B(\text{v}_{\text{GS}} > \text{V}_{T}) = \rule{2in}{0.1pt} \text{A}$$

Problem 2 continues on the next page
Problem 2 continued

(III) The device shown below is an isolated MOS capacitor. It is identical to the earlier structure with the n-region removed and the gate electrode covering the entire area.

In an isolated MOS capacitor there is no adjacent n-region to instantly supply the electrons to form the inversion layer, so if the gate voltage is abruptly changed from \( V_{FB} \) to \( V_T + 2V \), for example, at \( t = 0 \), there will be no inversion layer at \( t = 0^+ \), and the potential drop across the semiconductor depletion region will initially exceed \( 2|\phi_p| \). Eventually electrons will diffuse from the bulk silicon quasi-neutral region to the oxide-silicon interface under the gate, just as they did in Part g) of this problem. As these electrons collect at the interface the inversion layer will be populated, but it takes time.

h) [4 pts] What is the steady state charge density in the inversion layer, AND how long will it take for this inversion layer to form? **Note:** Your answers in Parts d) and g) of this problem should help you answer this question. If you could not answer those parts, you may write our answers here as algebraic expressions involving the quantities asked for in them.

Steady state sheet charge density in inversion layer: _______________ Coul/cm²

Time for inversion layer to form: _______________ s

i) [4 pts] The gate voltage in excess of the flatband voltage, \( (V_{GB} - V_{FB}) \), is equal to the sum of the electrostatic potential change across the depletion region, \( \Delta \phi_{DP} \), and the voltage drop across the oxide, \( \Delta V_{ox} \), i.e. \( (V_{GB} - V_{FB}) = \Delta V_{ox} + \Delta \phi_{DP} \). Write expressions for each of these factors at \( t = 0^+ \) (i.e., before there is any inversion layer charge). Use \( x_{dr} \), the width of the depletion region, as a variable in your expressions, but do not find \( x_{dr} \).

\[ \Delta V_{ox} = \______________ \]

\[ \Delta \phi_{DP} = \______________ \]

End of Problem 2
Problem 3 - (40 points)

This problem concerns the inverter shown below on the left, which uses an enhancement mode n-channel MOSFET as the switching, or "pull-down" device, and a depletion mode n-channel MOSFET as the load, or "pull-up" device. (Traditionally logic based on this type of inverter is called NMOS.)

To make life interesting, the NMOS inverter you are given to analyze is made with very short gate MOSFETs. The gates are so small (short) that velocity saturation is an issue and the electrons in the channel reach their saturation velocity at very low drain-to-source voltages. Their terminal characteristics are shown below to the right.

![Inverter Diagram]

\[ V_{DD} = 3V \]

a) [4 pts] Re-label the characteristics of the pull-down transistor below in terms of \( V_{IN} \) and \( V_{OUT} \) of the inverter, AND drawn the load line imposed on this device by the pull-up transistor.

Problem 3 continues on the next page

\* You do not need to know what "n-MOS" means or to what "velocity saturation" means to do most of this problem, so don't let this information scare you off. Ignore it and work the problem anyway!
Problem 3 continued

b) [4 pts] What is the value of $v_{OUT}$ when $v_{IN} = 0$ V? And, over what range of $v_{IN}$ does $v_{OUT}$ have this value?

\[ v_{OUT} \ (0 \leq v_{IN} \leq \ \text{Volts}) = \text{Volts} \]

c) [6 pts] There is a portion of the inverter transfer characteristic that is vertical (i.e., in the graph of $v_{OUT}$ vs $v_{IN}$ there is a value of $v_{IN}$ for which $v_{OUT}$ can have a range of values. What is this value of $v_{IN}$, and what is the range of possible values of $v_{OUT}$?

\[ v_{IN} = \ \text{Volts} \]
\[ \ \text{Volts} \leq v_{OUT} \leq \ \text{Volts} \]

d) [4 pts] What is the value of $v_{OUT}$ when $v_{IN} = V_{DD} (= 3$ V)?

\[ v_{OUT} \ (v_{IN} = 3 \text{ V}) = \ \text{Volts} \]

e) [4 pts] On the axes provided below, draw the transfer characteristic for this inverter. First plot your answers to Parts b), c), and d), and then sketch lines connecting those portions of the curve to form a continuous characteristic. Indicate the nature of the lines you sketch in (i.e. straight, convex up, etc.); you do not need to find expressions for them.

![Graph of vOUT vs vIN]

Problem 3 continues on the next page
Problem 3 continued

f) [4 pts] On the transfer characteristic you plotted in Part e) indicate $V_{HI}$ and $V_{LO}$ on the horizontal, $v_{IN}$, axis. Also indicate the high and low noise margins, $V_{NMH}$ and $V_{NML}$, respectively. If you could not do Part e), sketch a generic transfer characteristic and use it to answer this part.

g) [6 pts] On the axes provided below plot the charging and discharging currents, respectively, that flow into the load when the pull-down is turned off after having been on a long time, and that flow out of the load when it is turned on after having been off a long time.

![Graph showing current and voltage plots](image)

h) [4pts] Estimate the time required to charge a 1 pF ($= 1 \times 10^{-12}$ Farads) load to $V_{HI}$ when the pull-down is turned off after having been on a long time.

$$\tau_{ave} = \text{[time in seconds]}$$

i) [4pts] Assume that the two transistors in this inverter are identical, except for their different threshold voltages. What are these two threshold voltages, $V_{T,PU}$ and $V_{T,PD}$?

$$V_{T,PU} = \text{[value in volts]}$$

$$V_{T,PD} = \text{[value in volts]}$$

End of Problem 3 and of Exam Two