Announcements

In PS #9, P5 should refer to Foil 26 of Lec 19

Design Problem - coming out next week Wed.; PS #10 looks at pieces; neglect the Early effect in large signal analyses

Review - Single-transistor building block stages

- **Common source**: general purpose gain stage, workhorse
- **Common gate**: small $R_{in}$, large $R_{out}$, unity $A_i$, same $A_v$ as CS
- **Source follower**: large $R_{in}$, small $R_{out}$, unity $A_v$, same $A_i$ as CS
- **Series and Shunt feedback**: we'll see in special situations

Differential Amplifier Stages - Large signal behavior

- **General features**: symmetry, inputs, outputs, biasing (Symmetry is the key!)
- **Large signal transfer characteristic**

Difference- and common-mode signals

- Decomposing and reconstructing general signals

Half-circuit incremental analysis techniques

- **Linear equivalent half-circuits**
- **Difference- and common-mode analysis**
- **Example**: analysis of source-coupled pair
Linear amplifier layouts: The practical ways of putting inputs to, and taking outputs from, transistors to form linear amplifiers

There are 12 choices: three possible nodes to connect to the input, and for each one, two nodes from which to take an output, and two choices of what to do with the remaining node (ground it or connect it to something).

Not all these choices work well, however. In fact only three do:

<table>
<thead>
<tr>
<th>Name</th>
<th>Input</th>
<th>Output</th>
<th>Grounded</th>
</tr>
</thead>
<tbody>
<tr>
<td>Common source/emitter</td>
<td>1</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>Common gate/base</td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Common drain/collector (Source/emitter follower)</td>
<td>1</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>Source/emitter degeneration</td>
<td>1</td>
<td>2</td>
<td>none</td>
</tr>
</tbody>
</table>
• Three MOSFET single-transistor amplifiers

COMMON SOURCE
Input: gate
Output: drain
Common: source
Substrate: to source

COMMON GATE
Input: source; Output: drain
Common: gate
Substrate: to ground

SOURCE FOLLOWER
Input: gate
Output: source
Common: drain
Substrate: to source
- Single-transistor amplifiers with feedback

**PARALLEL FEEDBACK**

**SERIES FEEDBACK**

*Also termed "source degeneracy*
- Summary of the single transistor stages (MOSFET)

**MOSFET**

<table>
<thead>
<tr>
<th>Voltage gain, $A_v$</th>
<th>Current gain, $A_i$</th>
<th>Input resistance, $R_i$</th>
<th>Output resistance, $R_o$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$-\frac{g_m}{g_o + g_l} = -g_m R_i'$</td>
<td>$\infty$</td>
<td>$\infty$</td>
<td>$r_o = \frac{1}{g_o}$</td>
</tr>
<tr>
<td>$\approx [g_m + g_{mb}] r_i'$</td>
<td>$\approx 1$</td>
<td>$\approx \frac{1}{g_m + g_{mb}}$</td>
<td>$\approx r_o \left{ 1 + \frac{g_m + g_{mb} + g_o}{g_i} \right}$</td>
</tr>
<tr>
<td>$\frac{g_m}{g_m + g_{mb} + g_o + g_l} \approx 1$</td>
<td>$\infty$</td>
<td>$\infty$</td>
<td>$\approx \frac{1}{g_m}$</td>
</tr>
<tr>
<td>$\approx -\frac{r_i}{R_F}$</td>
<td>$\infty$</td>
<td>$\infty$</td>
<td>$r_o$</td>
</tr>
<tr>
<td>$\approx -\frac{g_{m}G_F}{g_o + G_F} \approx -g_m R_F - \frac{g_l}{G_F}$</td>
<td>$\frac{1}{G_F [1 - A_v]}$</td>
<td>$r_o \parallel R_F \left( \frac{1}{g_o + G_F} \right)$</td>
<td></td>
</tr>
</tbody>
</table>

**Power gain, $A_p = A_v \cdot A_i$**

**Note:** When $v_{bs} = 0$ the $g_{mb}$ factors should be deleted.
• Summary of the single transistor stages (bipolar)

BIPOLAR

<table>
<thead>
<tr>
<th>Common emitter</th>
<th>Voltage gain, ( A_v )</th>
<th>Current gain, ( A_i )</th>
<th>Input resistance, ( R_i )</th>
<th>Output resistance, ( R_o )</th>
</tr>
</thead>
<tbody>
<tr>
<td>- ( \frac{g_m}{g_o + g_l} ) ((-g_m r_i^{'}))</td>
<td>- ( \frac{\beta g_l}{g_o + g_l} )</td>
<td>( r_{\pi} )</td>
<td>( \frac{1}{g_o} )</td>
<td></td>
</tr>
<tr>
<td>( g_m ) (( g_m r_i^{'} ))</td>
<td>( \approx \frac{\beta g_l}{g_o + g_l} )</td>
<td>( \approx \frac{r_{\pi}}{\beta + 1} )</td>
<td>( \approx [\beta + 1]r_o )</td>
<td></td>
</tr>
<tr>
<td>( \frac{g_m}{g_o + g_l} ) (( g_m r_i^{'} ))</td>
<td>( \approx 1 )</td>
<td>( \approx r_{\pi} + [\beta + 1]r_i^{'} )</td>
<td>( \approx r_o )</td>
<td></td>
</tr>
<tr>
<td>( \frac{g_m + g_{\pi}}{g_m + g_{\pi} + g_o + g_l} ) (( \approx 1 ))</td>
<td>( \approx \beta )</td>
<td>( \approx r_{\pi} + [\beta + 1]R_F )</td>
<td>( \approx r_o )</td>
<td></td>
</tr>
<tr>
<td>( -\frac{r_i}{R_F} )</td>
<td>( \approx \beta )</td>
<td>( \approx r_{\pi} + [\beta + 1]R_F )</td>
<td>( \approx r_o )</td>
<td></td>
</tr>
<tr>
<td>( \frac{g_m - G_F}{g_o + G_F} ) (( \approx -g_m R_F ))</td>
<td>( \approx g_m R_F )</td>
<td>( \approx \beta )</td>
<td>( \approx r_o )</td>
<td></td>
</tr>
</tbody>
</table>

Emitter follower

<table>
<thead>
<tr>
<th>Shunt feedback</th>
<th>Voltage gain, ( A_v )</th>
<th>Current gain, ( A_i )</th>
<th>Input resistance, ( R_i )</th>
<th>Output resistance, ( R_o )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( -\frac{g_m - G_F}{g_o + G_F} ) (( \approx -g_m R_F ))</td>
<td>( \approx g_m R_F )</td>
<td>( \approx \beta )</td>
<td>( \approx r_o )</td>
<td></td>
</tr>
</tbody>
</table>

Power gain, \( A_p = A_v \cdot A_i \)
Differential Amplifiers: emitter- and source-coupled pairs

Emitter-coupled pair

Source-coupled pair

Why do we care? - They amplify only difference-mode signals
They are easy to interconnect and cascade
They help us eliminate coupling capacitors
They are optimally suited to integration
Differential Amplifiers: large signal analysis of source coupled pairs

Source-coupled pair

Below: Schematic with resistor loads
Right: Large signal equiv. circuit in saturation

Analysis:

3 KVL loops: \( v_{I1} - v_{GS1} + v_{GS2} - v_{I2} = 0, \) \( v_{O1} = V_{DD} - R_D i_{D1}, \) \( v_{O2} = V_{DD} - R_D i_{D2} \)

KCL at one node: \( i_{D1} + i_{D2} = I_{BIAS} \)

MOSFET relationships: \( i_{D1} = K(v_{GS1} - V_T)^2/2; \) \( i_{D2} = K(v_{GS2} - V_T)^2/2 \)

(see text for details of analysis)
**Diff. Amps:** large signal analysis of source coupled pairs, cont.

**Results:** The outputs again only depend on the difference between the two inputs, \((v_{i1} - v_{i2})\):

\[
v_{o1} = V_{DD} - \frac{R_D}{2} \left\{ K \left[ v_{IN1} - v_{IN2} \right]^2 + I_{BIAS} \right\} + \frac{K}{2} \left[ v_{IN1} - v_{IN2} \right] \sqrt{\frac{4I_{BIAS}}{K}} - \left[ v_{IN1} - v_{IN2} \right]^2
\]

\[
v_{o2} = V_{DD} - \frac{R_D}{2} \left\{ K \left[ v_{IN1} - v_{IN2} \right]^2 + I_{BIAS} \right\} - \frac{K}{2} \left[ v_{IN1} - v_{IN2} \right] \sqrt{\frac{4I_{BIAS}}{K}} - \left[ v_{IN1} - v_{IN2} \right]^2
\]

\[
v_{o} = -\frac{R_D K}{2} \left[ v_{IN1} - v_{IN2} \right] \sqrt{\frac{4I_{BIAS}}{K}} - \left[ v_{IN1} - v_{IN2} \right]^2
\]

Slope around origin = \(-g_m R_D\)

Only the difference in the inputs matters!!

Symmetrical
Differential Amplifiers: large signal analysis of emitter coupled pairs

Emitter-coupled pair

Below: Schematic with resistor loads
Right: Large signal equivalent circuit in FAR

Analysis:

3 KVL loops: \( v_{i1} - v_{BE1} + v_{BE2} - v_{i2} = 0 \), \( v_{O1} = V_{CC} - R_C \alpha_F i_{F1} \), \( v_{O2} = V_{CC} - R_C \alpha_F i_{F2} \)

KCL at one node: \( i_{F1} + i_{F2} = I_{BIAS} \)

Ideal diode relationships: \( i_{F1} \approx I_{ES} \exp \left( qv_{BE1}/kT \right) \), \( i_{F2} \approx I_{ES} \exp \left( qv_{BE2}/kT \right) \)

(see text for details of analysis)
**Diff. Amps:** large signal analysis of emitter coupled pairs, cont.

**Results:** The outputs only depend on the difference between the inputs, \((v_{i1} - v_{i2})\):

\[
v_{O1} = V_{CC} - \frac{\alpha \cdot R \cdot I_{BIAS}}{1 + e^{\frac{-q(v_{i1} - v_{i2})}{kT}}}
\]

\[
v_{O2} = V_{CC} - \frac{\alpha \cdot R \cdot I_{BIAS}}{1 + e^{\frac{q(v_{i1} - v_{i2})}{kT}}}
\]

\[
v_{O} = -\alpha \cdot R \cdot I_{BIAS} \tanh \left( \frac{q(v_{i1} - v_{i2})}{2kT} \right)
\]

**Symmetrical**

Slope around origin = \(-g_m R_C\)

Only the difference in the inputs matters!!
**Differential Amplifier Analysis** - difference-mode and common-mode signals

Any pair of signals can be decomposed into a portion that is the identical in both, and a portion that is equal, but opposite in both. For example, if we have two voltages, $v_1$ and $v_2$, we can define a common-mode signal, $v_C$, and a difference-mode signal, $v_D$, as:

$$v_C = \frac{(v_1 + v_2)}{2} \quad v_D = v_1 - v_2$$

In terms of these two voltages, we can write $v_1$ and $v_2$ as:

$$v_1 = v_C + \frac{v_D}{2} \quad v_2 = v_C - \frac{v_D}{2}$$

In incremental analysis of linear amplifiers we will decompose our inputs into difference- and common-mode inputs:

$$v_{ic} = \frac{(v_{in1} + v_{in2})}{2} \quad \text{and} \quad v_{id} = v_{in1} - v_{in2}.$$ 

We will apply $v_{id}$ to the circuit and get $v_{od}$ ($= A_{vd}v_{id}$), and then apply $v_{ic}$ to the circuit to get $v_{oc}$ ($= A_{vc}v_{ic}$). Then we will reconstruct our outputs:

$$v_{out1} = v_{oc} + \frac{v_{od}}{2} = A_{vc}v_{ic} + A_{vd}\frac{v_{id}}{2}$$

$$v_{out2} = v_{oc} - \frac{v_{od}}{2} = A_{vc}v_{ic} - A_{vd}\frac{v_{id}}{2}$$
Differential Amplifier Analysis -
incremental analysis exploiting symmetry and superposition

Linear equivalent circuit (symmetrical)

a LEHC: one half of sym. LEC

a LEHC: one half of sym. LEC

Clif Fonstad, 4/14/11

Lecture 19 - Slide 13
Differential Amplifier Analysis -
incremental analysis exploiting symmetry and superposition

\[ V_{od} = A_{vd} V_{id} \]

\[ V_{oc} = A_{vc} V_{ic} \]

No voltage on common links, so incrementally they are grounded.

No current in common links, so incrementally they are open.
Differential Amplifier Analysis - example of LEC analysis

Consider a source-coupled pair:

We begin by drawing the LEC for this differential amplifier....
Differential Amplifier Analysis - example, cont.

The LEC for our amplifier:

We decompose our inputs into common- and difference-mode inputs:

\[ v_{id} \equiv v_{in1} - v_{in2} \]
\[ v_{ic} \equiv \frac{v_{in1} + v_{in2}}{2} \]

Also:

\[ v_{od} \equiv v_{out1} - v_{out2} \]
\[ v_{oc} \equiv \frac{v_{out1} + v_{out2}}{2} \]
**Differential Amplifier Analysis** - example, cont.

**With** $v_{id}$ and $-v_{id}$ inputs:

\[ v_{od} = \frac{-g_m v_{id}}{g_o + g_{sl} + g_{el}} \]

\[ A_{vd} = \frac{-g_m}{g_o + g_{sl} + g_{el}} \]

**Note:** We want $A_{vd}$ to be very large.
Differential Amplifier Analysis - example, cont.

With \( v_{ic} \) inputs:

This LEC simplifies to:

\[
\begin{align*}
\text{From which:} \\
V_{oc} &\approx -\frac{g_{cs}v_{ic}}{2(g_{sl} + g_{el})} \\
A_{vc} &\approx -\frac{g_{cs}}{2(g_{sl} + g_{el})}
\end{align*}
\]

Note: We want \( A_{vc} \) to be very small.
Differential Amplifier Analysis - example, cont.

Knowing $A_{vd}$ and $A_{vc}$, we can construct $v_{o1}$ and $v_{o2}$:

$$v_{o1} = v_{oc} + \frac{v_{od}}{2} = A_{vc}v_{ic} + \frac{A_{vd}v_{id}}{2}$$

$$= -\frac{g_{cs}}{2(g_{sl} + g_{el})}v_{ic} - \frac{g_{m}}{2(g_{o} + g_{sl} + g_{el})}v_{id}$$

$$= -\frac{g_{cs}}{2(g_{sl} + g_{el})} \left(\frac{v_{i1} + v_{i2}}{2}\right) - \frac{g_{m}}{2(g_{o} + g_{sl} + g_{el})}(v_{i1} - v_{i2})$$

$$v_{o2} = v_{oc} - \frac{v_{od}}{2} = A_{vc}v_{ic} - \frac{A_{vd}v_{id}}{2}$$

$$= -\frac{g_{cs}}{2(g_{sl} + g_{el})}v_{ic} + \frac{g_{m}}{2(g_{o} + g_{sl} + g_{el})}v_{id}$$

$$= -\frac{g_{cs}}{2(g_{sl} + g_{el})} \left(\frac{v_{i1} + v_{i2}}{2}\right) + \frac{g_{m}}{2(g_{o} + g_{sl} + g_{el})}(v_{i1} - v_{i2})$$

**Remember:** In a good Diff Amp $|A_{vd}|$ is very large, and $|A_{vc}|$ is very small.
Looking at a complicated circuit:
Lesson I - Find the biasing circuitry and represent it symbolically

Consider the following example:

8 of the 24 transistors are used for biasing the other 16 transistors.
If we get the biasing transistors out of the picture for awhile, the circuit looks simpler. (next foil)
Looking at a complicated circuit:
Lesson II - Identify the individual stages and their active transistors and load elements.

Continuing with our earlier example, consider the following:

**Push-Pull Output Stage (bipolar)**

**Source-coupled pair**

**Pair of common-source stages**

**Complementary emitter follower pair (pnp and npn)**

**Actives**

**Loads**

Note: We can almost make sense of all of the stages, but we still need to study active loads and output stages to fully understand them.
Looking at a complicated circuit:
Lesson III - Use half-circuit techniques to convert the differential stages to familiar single transistor stages.

Continuing with the same example:

There are two symmetrical differential gain stages, followed by two complementary output stages (next foil)
Looking at a complicated circuit:

Lesson III, cont. - Draw the difference and common mode half circuits.

Voila!! We have reduced the transistor count from 24 to 4, and we see that our complex amplifier is just a cascade of 4 single-transistor stages.
6.012 - Microelectronic Devices and Circuits

Lecture 19 - Differential Amplifier Stages - Summary

• Differential Amplifier Stages - Large signal behavior
  General features: two transistors (a source-coupled, or emitter-coupled, pair)
  highly symmetrical
  two inputs, two outputs (Note: one input can be zero)
  biased by single current source

Large signal transfer characteristic: only depends on $v_{IN1} - v_{IN2}$

• Difference- and common-mode signals
  Difference-mode: $v_{ID} = v_{IN1} - v_{IN2}$
  Common-mode: $v_{IC} = (v_{IN1} + v_{IN2})/2$
  Reconstruction: $v_{IN1} = v_{ID} + v_{IC}/2$, $v_{IN2} = v_{ID} - v_{IC}/2$

• Half-circuit incremental analysis techniques
  Exploiting symmetry and superposition
  Difference-mode lin. equiv. half-circuit: links are grounded
  Common-mode lin. equiv. half circuit: links are cut, open circuited
  Approach: 1. identify common- and difference-mode half circuits
  2. calculate common- and difference-mode signals
  3. analyze difference-mode half-circuit
  4. analyze common-mode half-circuit
  5. reconstruct signals

(each half-circuit is one of our known building-blocks)