Lesson I - Find the biasing circuitry and represent it symbolically

8 of the 24 transistors are used for biasing the other 16 transistors.
If we get the biasing transistors out of the picture for awhile, the circuit looks simpler. (next foil)
Looking at a complicated circuit:
Lesson II - Identify the individual stages and their active transistors and load elements.

Continuing with our earlier example, consider the following:

Note: We can almost make sense of all of the stages, but we still need to study active loads and output stages to fully understand them.
Looking at a complicated circuit:

Lesson III - Use half-circuit techniques to convert the differential stages to familiar single transistor stages.

Continuing with the same example:

There are two symmetrical differential gain stages, followed by two complementary output stages (next foil)
Looking at a complicated circuit:

Lesson III, cont. - Draw the difference and common mode half circuits.

Voila!! We have reduced the transistor count from 24 to 4, and we see that our complex amplifier is just a cascade of 4 single-transistor stages.
A constraint on the bias currents is the total power dissipation specification of 7.5 mW. This means that the total bias current must be \( \approx 2.5 \) mA or less (i.e, \( 3 \text{ V} \times 2.5 \text{ mA} = 8.5 \) mW).

\[
P_Q = \left(I_A + I_B + I_C + I_D + I_E + I_F\right) \times 3 \text{ Volts}
\]

\[
I_A + I_B + I_C + I_D + I_E + I_F \leq 2.5 \text{ mA}
\]
**Differential Amplifiers - common-mode input range**

\( (V_{C,\text{min}} \leq v_C \leq V_{C,\text{max}}) \)

We have said the output changes very little for common-mode inputs. This is true as long as the \( v_C \) doesn't push the transistors out of saturation.

There are a minimum and maximum \( v_C \):

- \( V_{C,\text{max}} \): As \( v_C \) increases, \( v_{DS9} \) and \( v_{DS10} \) decrease until \( Q_9 \) and \( Q_{10} \) are no longer in saturation.

- \( V_{C,\text{min}} \): As \( v_C \) decreases, \( v_{DS11} \) decreases until \( Q_{11} \) is no longer in saturation.

**Key thing to see:** The node between \( Q_9/Q_{10} \) and \( Q_{11} \) moves up and down with \( v_C \).
Differential Amplifiers - output voltage range

\[ V_{\text{OUT,min}} \leq v_{\text{OUT}} \leq V_{\text{OUT,max}} \]

As \( v_{\text{OUT}} \) goes down, \( Q_{16} \) and/or \( Q_{22} \) may go out of saturation; as \( v_{\text{OUT}} \) goes up, the same may happen to \( Q_{14} \) and/or \( Q_{19} \).
The first two stages are gain stages with “active” loads. The first has a Lee Load (Slides 8 thru 14), and the second has a Current Mirror Load (Slides 15 thru 17).

**Active Loads - The Lee load**

A load for a fully-differential stage that looks like a large resistance in difference-mode and small resistance in common-mode.

The conventional schematic is drawn here, but the coupling of the load and what is happening is made clearer by redrawing the circuit (next slide.)
Active Loads - The Lee load. cont.

Drawn as on the right we see that the load MOSFETs on each side are driven by both outputs. The result is different if the two outputs are equal and opposite (diff-mode operation) or if they are equal (common-mode). The next few slides give the results for each mode.

Drawn to highlight cross-coupling and demonstrate symmetry.
The Lee load: analysis for difference-mode inputs

LEHC: difference-mode

\[ v_{id}/2 = v_{gs5} \]

\[ g_{m5} v_{id}/2 \]

\[ g_{o5} \]

\[ g_{m1} v_{od}/2 \]

\[ g_{o1} \]

\[ -g_{m3} v_{od}/2 \]

\[ g_{o3} \]

\[ v_{od}/2 \]

\[ g_{el} \]

\[ g_{oLLLd} \]
The Lee load: analysis for difference-mode inputs, cont

LEHC: difference-mode

\[ v_{id}/2 = v_{gs5} \]

\[ v_{id}/2 = v_{gs} \]

\[ v_{id}/2 = v_{gs} \]

\[ g_{o5} \]

\[ g_{m5} v_{id}/2 \]

\[ g_{m1} v_{od}/2 \]

\[ g_{o1} \]

\[ -g_{m3} v_{od}/2 \]

\[ g_{o3} \]

\[ v_{od}/2 \]

\[ g_{el} \]

\[ g_{oLLd} = 2 g_{o1} \]

\[ A_{vd} = \frac{v_{od}}{v_{id}} = \frac{-g_{m5}}{g_{o5} + 2g_{o1} + g_{el}} \]

Note: In D.P., the outputs go to MOSFET gates so \( g_{el} = 0 \).
The Lee load: analysis for common-mode inputs

LEHC: common-mode
The Lee load: analysis for common-mode inputs, cont

LEHC: common-mode

\[ g_{oLLc} = 2(g_{m1} + g_{o1}) \approx 2g_{m1} \]

\[ A_{vc} = \frac{v_{oc}}{v_{ic}} = \frac{-g_{ob}}{2[2(g_{m1} + g_{o1}) + g_{e1}]} \approx -\frac{g_{ob}}{4g_{m1}} \]

Note: In D.P., the outputs go to MOSFET gates so \( g_{el} = 0 \).
The Lee load: applying these results to the Design Problem

\[ Q_n \rightarrow Q_{n+4}, \quad g_{el} = 0, \quad I_{BIAS} = I_{BIAS1}, \quad g_{ob} \rightarrow g_{o11} \]

**Difference-mode Gain**

\[
A_{vd} = \frac{v_{od}}{v_{id}} = \frac{-g_{m9}}{\left(g_o9 + 2g_o5\right)} = -\frac{2\left(I_{BIAS1}/2\right)}{\left(V_{GS9} - V_T\right)} = -\frac{2}{\left(V_{GS9} - V_T\right)} \left(\frac{1}{V_{A9}} + \frac{1}{V_{A5}}\right)
\]

**Common-mode Gain**

\[
A_{vc} = \frac{v_{oc}}{v_{ic}} = \frac{-\left(g_{o11}/2\right)}{2\left(g_m5 + g_o5\right)} \approx -\frac{g_{o11}}{4g_m5} = -\frac{I_{BIAS1}}{V_{A11}} = -\frac{\left(V_{SG5} - |V_T|\right)}{2V_{A11}}
\]

**Overall**

\[
\frac{\left(v_{out1,s1} - v_{out2,s1}\right)}{2} = -\frac{2}{\left(V_{GS9} - V_T\right)} \left(V_{A5} + V_{A9}\right) \left(v_{in1} - v_{in2}\right)
\]

\[
\frac{\left(v_{out1,s1} + v_{out2,s1}\right)}{2} = -\frac{\left(V_{SG5} - |V_T|\right)}{2V_{A11}} \left(v_{in1} + v_{in2}\right)
\]
Active Loads: The current mirror load

Large differential-mode gain, small common-mode gain. Also provides high gain conversion from double-ended to single-ended output.

The circuit is no longer symmetrical, so half-circuit techniques can not be applied. The full analysis is found in the course text. We find:

**Difference-mode inputs**

\[ v_{out,d} = \frac{2g_{m3}}{g_{o2} + g_{o4} + g_{el}} \frac{v_{id}}{2} \]
Active Loads: The current mirror load, cont.

Common-mode inputs

\[ v_{out,c} = \frac{g_{ob}}{2g_{m2}} v_{ic} \]

With both inputs:

\[ v_{out} = \frac{2g_{m3}}{(g_{o2} + g_{o4} + g_{el})} \left( \frac{v_{in1} - v_{in2}}{2} \right) - \frac{g_{ob}}{2g_{m2}} \left( \frac{v_{in1} + v_{in2}}{2} \right) \]

Note: In D.P. the output goes to the gate of a BJT; \( g_{el} \) matters.
Current mirror load: application to the Design Problem

\[
g_{o12} = \frac{I_{BIAS2}}{V_{A12}}, \quad g_{m17} = g_{m18} = \frac{2(I_{BIAS2}/2)}{(V_{GS17} - V_T)} = \frac{I_{BIAS2}}{(V_{GS17} - V_T)}
\]

Ground in Diff mode; open in Common.
**Current mirror load:** application to the Design Problem

\[ Q_1 \rightarrow Q_{15}, \ Q_2 \rightarrow Q_{16}, \ Q_3 \rightarrow Q_{13}, \ Q_4 \rightarrow Q_{14}, \ g_{ob} \rightarrow g_{o12}, \ I_{BIAS} = I_{BIAS2} \]

**Total output** (Note: these inputs are stage inputs, not amplifier inputs)

\[
v_{out,s2} = \frac{2g_{m14}}{\left(g_{o16} + g_{o14} + g_{el}\right)} \left(\frac{v_{in1,s2} - v_{in2,s2}}{2} \right) - \frac{g_{o12}}{g_{m16}} \left(\frac{v_{in1,s2} + v_{in2,s2}}{2}\right)
\]

\[
= \frac{2 \left(\frac{I_{BIAS2}}{2}\right)}{\left(V_{SG14} - |V_T|\right)} \left(\frac{v_{in1,s2} - v_{in2,s2}}{2}\right) - \frac{I_{BIAS2}}{V_{A12}} \left(\frac{v_{in1,s2} + v_{in2,s2}}{2}\right)
\]

\[
= \frac{4}{\left(V_{SG14} - |V_T|\right)} \left(\frac{v_{in1,s2} - v_{in2,s2}}{2}\right) - \frac{V_{GS16} - V_T}{V_{A12}} \left(\frac{v_{in1,s2} + v_{in2,s2}}{2}\right)
\]

* Note: 2 \( g_{m2} \) is replaced by \( 2(1/g_{m16} + 1/g_{m18})^{-1} = ** g_{m16}, \) because in common-mode \( Q_{16} \) and \( Q_{18} \) are in series.

6.012 Design Problem

(** This equality is of course only valid if \( Q_{16} \) and \( Q_{18} \) are identical.)
Specialty Pairings: The Push-pull or Totem Pole Output

A stacked pair of complementary emitter- or source-followers

- Large input resistance
- Small output resistance
- Voltage gain near one
- Low quiescent power

npn or n-MOS follower

pnp or p-MOS follower

\[ V^+ \]
\[ Q_n \]
\[ V^- \]
\[ + \]
\[ - \]
\[ v_{in} + V_{BE_n} \]
\[ v_{in} - V_{EB_p} \]
\[ v_{out} \]
\[ R_L \]

\[ V^+ \]
\[ Q_n \]
\[ V^- \]
\[ + \]
\[ - \]
\[ v_{in} + V_{GS_n} \]
\[ v_{in} - V_{SG_p} \]
\[ v_{out} \]
\[ R_L \]
Specialty pairings: Push-pull or Totem Pole Output Pairs

The limitations of using a simple follower stage* output:
- Using a single source follower as the output stage must be biased with a relatively large drain current to achieve a large output voltage swing, which in turn dissipates a lot of quiescent power.

* source follower or emitter follower
Specialty pairings: Push-pull or Totem Pole, cont.

- A p-MOS follower solves the negative swing problem, but has its own positive swing problem.

- The solution is to combine the two in a totem pole stack (and drive and bias them by the preceding stage).

As $Q$ turns off, $I_{BIAS}$ flows through load.

$v_{IN}$ goes positive.

$v_{OUT}$ swing limited to $I_{BIAS}R_L$.

$Q_3$ and $Q_4$ bias $Q_2$ and $Q_5$. They also insure that $Q_5$ turns off as $Q_2$ turns on, and visa versa.

$Q_2$ supplies the load current for $v_{OUT} > 0$.

$Q_5$ sinks the load current for $v_{OUT} < 0$. 

$v_{IN}$ turns off $Q$.

$V_-$

$I_{BIAS}$

$+ 1.5 \text{ V}$

$- 1.5 \text{ V}$

$V_+$
Specialty pairings: Push-pull or Totem Pole, cont.

Comments/Observations:
- The output resistance is largest around $v_{\text{OUT}} = 0$. Here both $Q_2$ and $Q_5$ are active and the output resistance is:

$$r_{\text{out}} \approx \frac{1}{g_{m2} + g_{m5}}$$

- One must always make $K_2/K_3 = K_5/K_4$, and in the typical design $K_3 = K_4$, and $K_2 = K_5$.

The bias current of $Q_2$ and $Q_5$ is set by $I_{\text{BIAS}}$:

$$I_{D2} = I_{D5} = \left(\frac{K_2}{K_3}\right)I_{\text{BIAS}}$$

- $|v_{\text{OUT}}|$ vs $|v_{\text{IN}}|$ is fairly linear over a wide range (see right); $|v_{\text{GS}}|$ increases slowly with $|v_{\text{IN}}|$.
Specialty pairings:  Push-pull or Totem Pole in Design Prob.

Comments/Observations:
- The D.P. output stage involves four emitter follower building blocks arranged as two parallel cascades of two emitter follower stages each.

- Driving the totem pole in this manner results in a much larger output voltage range than is obtained by using a single follower as was done in our earlier examples.

NOTE: Designing with this output requires paying special attention to the biasing, and calculating the input and output resistances.

The next several slides look at these aspects of the push-pull stage.
Specialty pairings:  Push-pull or Totem Pole in D.P., cont.

Biasing the output stages: getting the currents right

1. Constraint at input node:  \( I_{B21} = -I_{B20} \)
   Equivalently:  \( I_{E21}/(\beta_n + 1) = -I_{E20}/(\beta_p + 1) \)

2. Constraint at output node:  \( I_{E24} = -I_{E23} \)

3. Sum at emitter of \( Q_{20} \):
   \[
   I_{BIAS3} = I_{E20} - I_{E23}/(\beta_n + 1)
   = -(\beta_p + 1)I_{B20} - I_{E23}/(\beta_n + 1)
   = (\beta_p + 1) \left[ -I_{B20} + \frac{-I_{E23}}{(\beta_n + 1)(\beta_p + 1)} \right]
   \]

4. Sum at emitter of \( Q_{21} \):
   \[
   I_{BIAS4} = (\beta_n + 1)I_{21} + I_{E24}/(\beta_p + 1) = (\beta_n + 1) \left[ I_{B21} + \frac{I_{E24}}{(\beta_n + 1)(\beta_p + 1)} \right]
   \]

5. Combining everything:
   \[
   \frac{I_{BIAS2}}{I_{BIAS3}} = (\beta_p + 1)/(\beta_n + 1) \approx \beta_p/\beta_n
   \]

Lesson: The bias currents are constrained.
**Specialty pairings:** Push-pull or Totem Pole in D.P., cont.

Biasing the output stages: getting the voltages right

**KVL constraint:**

\[ V_{BE23} + V_{EB24} - V_{BE21} - V_{EB20} = 0 \]

**Relating voltages to currents:**

\[ V_{EB20} = \left( \frac{kT}{q} \right) \ln \left[ \frac{I_{E20}}{\gamma_{20} I_{ESP}} \right] \]
\[ V_{BE21} = \left( \frac{kT}{q} \right) \ln \left[ -\frac{I_{E21}}{\gamma_{21} I_{ESn}} \right] \]
\[ V_{BE23} = \left( \frac{kT}{q} \right) \ln \left[ -\frac{I_{E23}}{\gamma_{23} I_{ESn}} \right] \]
\[ V_{BE24} = \left( \frac{kT}{q} \right) \ln \left[ \frac{I_{E24}}{\gamma_{24} I_{ESP}} \right] \]

Combining everything, including the fact that \( I_{ESP} = I_{ESn} = I_{ES} \), and the results \( I_{E24} = -I_{E23} \) and \( I_{E20}/(\beta_p + 1) = -I_{E21}/(\beta_n + 1) \), yields:

\[ \frac{I_{E23}}{I_{E21}} = \sqrt{\frac{(\beta_p + 1) \gamma_{23} \gamma_{24}}{(\beta_n + 1) \gamma_{20} \gamma_{21}}} \]

**Lesson:** The BJT areas must be properly designed.
Specialty pairings: Push-pull or Totem Pole in D.P., cont.

Reviewing the input and output resistances of an emitter follower:

\[ r_{in} = r_{\pi} + (\beta + 1)(r_l \parallel r_o \parallel r_{Bias}) \]

\[ r_{in} \approx r_{\pi} + (\beta + 1)r_l \]

\[ r_{out} = \frac{1}{[g_o + g_{Bias} + (\beta + 1)/(r_{\pi} + r_t)]} \]

\[ r_{out} \approx (r_{\pi} + r_t)/(\beta + 1) \]

The only two things you need to know:
- Looking in the resistance is multiplied by \((\beta+1)\); looking back it is divided by \((\beta+1)\).
Specialty pairings: Push-pull or Totem Pole in D.P., cont.

Reviewing the voltage gain of an emitter follower:

\[ i_{in} = i_b \]

\[ v_{out} = (\beta + 1)i_b (r_l \parallel r_o \parallel r_{Bias}) \]

\[ v_{in} = i_b r_\pi + (\beta + 1)i_b (r_l \parallel r_o \parallel r_{Bias}) \]

\[ A_v = \frac{v_{out}}{v_{in}} = \frac{(\beta + 1)(r_l \parallel r_o \parallel r_{Bias})}{r_\pi + (\beta + 1)(r_l \parallel r_o \parallel r_{Bias})} \]

\[ A_v \approx \frac{(\beta + 1)r_l}{r_\pi + (\beta + 1)r_l} = \frac{r_l}{r_\pi/(\beta + 1) + r_l} = \frac{r_l}{1/g_m + r_l} \]

Note: The voltage gains of the third-stage emitter followers (Q_{17} and Q_{18}) will likely be very close to one, but that of the stage-four followers might be noticeably less than one.
Specialty pairings: Push-pull or Totem Pole in D.P., cont.

Operation: The npn follower supplies current when the input goes positive to push the output up, while the pnp follower sinks current when the input goes negative to pull the output down.

NOTE: Near $v_{in} = 0$ we have two paths in parallel, and this must be considered when finding $r_{in}$ and $r_{out}$. 
Specialty pairings: Push-pull or Totem Pole in D.P., cont.
The input resistance of the output stages as seen by the Current Mirror

We will make the approximation that the two emitter-follower paths can be modeled as being in parallel for purposes of calculating the input resistance.

Note: $r_{in}$ is smallest around $v_{in} = 0$, so this is a worst-case estimate.
Specialty pairings: Push-pull or Totem Pole in D.P., cont.

The output resistance of the amplifier as seen by the 50 Ω load

We will make the approximation that the two emitter-follower paths can be modeled as being in parallel for purposes of calculating the output resistance.

\[ r_{\text{out}} \approx r_{\text{out1}} \parallel r_{\text{out2}} \]

Note: \( r_{\text{out}} \) is largest around \( v_{\text{out}} = 0 \), so this is a worst-case estimate.
Push-Pull Stage Gain: application to the Design Problem

\[
\begin{align*}
\frac{r_{\pi 23}}{(\beta_p + 1)(\beta_n + 1)} &= \frac{1}{g_{m23}} = \frac{1}{g_{m24}} = \frac{r_{\pi 24}}{(\beta_n + 1)} \\
\frac{r_{\pi 23}}{(\beta_p + 1)} &= \frac{1}{g_{m23} + g_{m24}} = \frac{1}{2g_{m23}}
\end{align*}
\]

\[
A_{v,s4} = \frac{v_{out,s4}}{v_{in,s4}} \approx \frac{50}{50 + 1/2g_{m23}} = \frac{50}{50 + V_{th}/2I_{C23}}
\]
Specialty pairings: Push-pull or Totem Pole, cont.

Voltage gain:
- The design problem uses a bipolar totem pole. The gain and linearity of this stage depend on the bias level of the totem pole. The gain is higher for with higher bias, but the power dissipation is also.

To calculate the large signal transfer characteristic of the bipolar totem pole we begin with $v_{OUT}$:

$$v_{OUT} = R_L\left(-i_{E23} - i_{E24}\right)$$

The emitter currents depend on $(v_{IN} - v_{OUT})$:

$$i_{E23} = -I_{E23}e^{(v_{IN} - v_{OUT})/V_t}, \quad i_{E24} = I_{E24}e^{-(v_{IN} - v_{OUT})/V_t}$$

Putting this all together, and using $I_{E24} = -I_{E23}$, we have:

$$v_{out} = R_L I_{E23}\left(e^{(v_{IN} - v_{OUT})/V_t} - e^{-(v_{IN} - v_{OUT})/V_t}\right)$$

$$= 2 R_L I_{E23} \sinh\left(\frac{v_{IN} - v_{OUT}}{V_t}\right)$$

We can do a spread-sheet solution by picking a set of values for $(v_{IN} - v_{OUT})$, using the last equation to calculate the $v_{OUT}$, using this $v_{OUT}$ to calculate $v_{IN}$, and finally plotting $v_{OUT}$ vs $v_{IN}$. The results are seen on the next slide.
Voltage gain, cont.:
- With a 50 $\Omega$ load and for several different bias levels we find:

The $A_v$ is lowest and $r_{out}$ is highest at the bias point (i.e., $V_{IN} = V_{OUT} = 0$). $r_{in}$ to the stage is also lowest there.

The gain and linearity are improved by increasing the bias current, but the cost is increased power dissipation.
Design Problem Stage Gains: Collected gain equations

Stage 1:
\[
\frac{v_{out1,s1} - v_{out2,s1}}{2} = -\frac{-g_{m9}}{g_{o9} + 2g_{o5}} \cdot \frac{v_{in1} - v_{in2}}{2}
\]
\[
\frac{v_{out1,s1} + v_{out2,s1}}{2} = -\frac{g_{o11}}{4g_{m5}} \cdot \frac{v_{in1} + v_{in2}}{2}
\]

Stage 2:
\[
v_{out,s2} = \frac{2g_{m14}}{g_{o16} + g_{o14} + g_{el}} \cdot \frac{v_{out1,s1} - v_{out2,s1}}{2} - \frac{g_{o12}}{g_{m16}} \cdot \frac{v_{out1,s1} + v_{out2,s1}}{2}
\]

Stage 3:
\[
v_{out,s3} = \frac{(\beta_p + 1)[r_{\pi 23} + (\beta_n + 1)2R_L]}{r_{\pi 20} + (\beta_p + 1)[r_{\pi 23} + (\beta_n + 1)2R_L]} \cdot \frac{v_{out,s2}}{2}
\]

Stage 4:
\[
v_{out} \approx \frac{R_L}{1/2g_{m23} + R_L} \cdot \frac{g_{m14}}{g_{o16} + g_{o14} + g_{el}} \cdot \frac{g_{m9}}{g_{o9} + 2g_{o5}} \cdot \frac{v_{in1} - v_{in2}}{2}
\]

Overall:
\[
v_{out} \approx A_{vd} + A_{vc}
\]

\[A_{vd} = \frac{R_L}{1/2g_{m23} + R_L} \cdot \frac{g_{m14}}{g_{o16} + g_{o14} + g_{el}} \cdot \frac{g_{o12}}{g_{m16}} \cdot \frac{g_{o11}}{4g_{m5}} \cdot \frac{v_{in1} + v_{in2}}{2}
\]

\[A_{vc} = \frac{R_L}{1/2g_{m23} + R_L} \cdot \frac{g_{m9}}{g_{o9} + 2g_{o5}} \cdot \frac{v_{in1} - v_{in2}}{2}
\]
DC off-set at the output of an Operational Amplifier:

DC off-set:
The node between $Q_{14}$ and $Q_{16}$ is a high impedance node whose quiescent voltage can only be determined by invoking symmetry.

The voltage on these two nodes is equal if there is no input, i.e. $v_{IN1} = v_{IN2} = 0$, and if the circuit is truly symmetrical/matched.

In any practical Op Amp, a very small differential input, $v_{IN1} - v_{IN2}$, is required to make the voltage on this node (and $V_{OUT}$) zero.

**Assuming ideal matching.
DC off-set at the output of an Op Amp, cont:

\[ V_{\text{HIN}} (-0.2 \text{ V}) \]

\[ A_{v3}A_{v4}V_{\text{HIN}} (-0.18 \text{ V}) \]

\[ A_{vd1}A_{vd2} (-10,000) \]

\[ A_{v3}A_{v4} (0.9) \]

\[ \frac{V_{\text{HIN}}}{A_{vd1}A_{vd2}} (20 \mu\text{V}) \]

\[ \frac{V_{\text{HIN}}}{A_{vd1}A_{vd2}} (20 \mu\text{V}) \]

\[ V_{\text{OUT}} = 2 \frac{V_{\text{HIN}}}{A_{vd1}A_{vd2}} (40 \mu\text{V}) \]
DC off-set at the output of an Op Amp, cont:

DC off-set:

The transfer characteristic, $v_{OUT}$ vs $(v_{IN1} - v_{IN2})$, will not in general go through the origin, i.e.,

$$v_{OUT} = A_{vd}(v_{IN1} - v_{IN2}) + V_{OFFSET}$$

In the example in the figure $A_{vd}$ is $-2 \times 10^6$, and $V_{OFFSET}$ is 0.1 V.

In a practice, an Op Amp will be used in a feed-back circuit like the example shown to the left, and the value of $v_{OUT}$ with $v_{IN} = 0$ will be quite small. For this example (in which $A_{vd} = -2 \times 10^6$, and $V_{OFFSET} = 0.1$ V), $v_{OUT}$ is only 0.1 $\mu$V.

In the D.P. you are asked for this value for your design.
**V_{REF} MOSFET diode stack:**

\[ +1.5\text{ V} \]

\[ \begin{align*}
Q_1 & \quad A \\
Q_2 \\
Q_3 \\
Q_4 & \quad B \\
-1.5\text{ V}
\end{align*} \]

**Constraints:**

\[
\begin{align*}
|V_{GS1}| + |V_{GS2}| + |V_{GS3}| + |V_{GS4}| &= 3.0\text{V} \\
K_1|V_{GS1} - V_{T1}|^2 &= K_2|V_{GS2} - V_{T2}|^2 \\
&= K_3|V_{GS3} - V_{T3}|^2 = K_4|V_{GS4} - V_{T4}|^2 \\
L_{\text{min}} &\leq L_i \leq 4L_{\text{min}} \\
W_{\text{min}} &\leq W_i \leq 50W_{\text{min}}
\end{align*}
\]

**Approach:**

Choose trial values for the \(v_{GSi}\)'s.

Use \(v_{GSi}\)'s to relate \(K_i\)'s.

Select n- or p-channel MOSFETs for \(Q_2\) and \(Q_3\).

Select \(L_i\)'s and \(W_i\)'s to satisfy \(K_i\) relationships.

Repeat if necessary to optimize design, e.g.

- minimizing sum of \(W_iL_i\) products, and/or
- minimizing bias current.