MASSACHUSETTS INSTITUTE OF TECHNOLOGY  
Department of Electrical Engineering and Computer Science  
6.012 Microelectronic Devices and Circuits – Spring 2011

SPECIAL PROBLEM ON CIRCUIT DESIGN – 4/28/11 edition


Due: Friday, May 6, 2011 in Room 13-3050 and on Stellar by 5 pm (be sure that your name is checked off the master list as you hand in your solution). Late solutions will receive zero points; see I.5 below.

Updates: Issues will be dealt with as needed; watch your e-mail.

I. General Comments

Do not panic when you see the circuit. It looks overwhelming at first but it is made up of simple building-block pieces and it is understandable. In addition, you will be given help along the way, first by this write-up, and later in recitations, lectures, and additional handouts. At the same time, the design process you need to go through is a complex one and it is not one you will successfully negotiate in one sitting. Thus it is important that you get started, first developing an understanding of the circuit and the nature of the design challenge, and then at doing your design. You can do it, but not in one night.

II. The Ground Rules

1. Consider this design problem more like an open book exam, than a problem set. You are encouraged to consult references and to seek guidance from the 6.012 staff, and to discuss design issues with others, but you should not work on your specific design and write-up with any other students or any other individuals. Nor should you compare design values or performance results with other students. The design you submit must be your own; any collaborations (and they should be minor) should be noted.

2. Do not let the design slide until the last week. Make a first attempt at a solution early so you can obtain any clarification and guidance you may need from the 6.012 staff well before the due date, May 6.

3. You are required to submit a completed Excel-file cover sheet, and a detailed discussion of your design and your approach to arriving at it. The Excel-file cover sheet will be available on Stellar. Your write-up should include circuit diagrams for your large signal and incremental analyses, and the equations you used and calculations you made. It should also include a discussion of the trade-offs you considered in your design. View the minimum performance objectives as a challenge and try to do even better.

4. Make reasonable approximations. Do not carry your calculations out to any more than three (3) significant figures. Your predicted performance values should also be stated to no more than three (3) significant figures. The following are examples of numbers with three significant figures: 1.23, 0.123, 123, 3450, 0.0345, 6.78 x 10^9.
5. Anyone who does not submit a design problem solution which demonstrates a reasonable level of effort will automatically receive zero points and a grade of "I" for 6.012 (as long as their performance is otherwise passing). This incomplete can only be completed by submitting an acceptable solution to this term’s design problem by July 15, 2011. Late solutions will be checked to determine that they are acceptable, but will receive zero points for purposes of determining an overall course grade.

III. Design Objective

Your design objective is to specify transistor dimensions for the integrated linear amplifier shown in Figure 1 on Page 3 so that it meets or, hopefully, exceeds the performance objectives itemized below. You are able to increase MOSFET gate widths and/or lengths and BJT areas by integer multiples.

The circuit, which is described in full detail in Section V, is a BiCMOS differential amplifier designed to have a large differential-mode gain, large common-mode rejection ratio, large common mode input voltage range, and large output voltage swing.

You are to specify the dimensions of the devices in the circuit in Figure 1, and to calculate the corresponding bias levels and performance characteristics. You are also expected to discuss the main aspects of your design in your solution write-up, and to also discuss there the factors you took into consideration in arriving at your design.

Performance Objectives:

1) Small signal gains defined by writing $v_{out} = A_{vd}(v_{in1}+v_{in2})/2 + A_{vd}(v_{in1}-v_{in2})$
   a) Small-signal differential-mode voltage gain, $A_{vd}$, with a 50 Ω load: as large as possible, and not less than 7,000
   b) Small-signal common-mode voltage gain, $A_{vc}$, with a 50 Ω load: as small as possible, and not more than $2 \times 10^{-5}$

2) Common-mode rejection ratio, $A_{vd}/A_{vc} : \geq 1 \times 10^{8}$

3) Small-signal output resistance, $r_{out} : \leq 15 \Omega$

4) Output voltage swing into a 50 Ω load, $v_{OUT} :$ at least ± 0.6 V

5) Common-mode input voltage range, $v_{IC} :$ at least ± 0.7 V

6) Total quiescent power dissipation not to exceed 7.5 mW

7) Offset Voltage, i.e. the quiescent voltage at the output, i.e. $v_{OUT}$, when connected in a feedback circuit like that illustrated below when $v_{IN} = 0$ (assuming perfect element matching): $|V_{OUT}| \leq 80 \mu V$
Figure 1 - The Spring 2011 Design Problem circuit, a high gain BICMOS differential amplifier with enhanced common-mode rejection ratio.
IV. **Component Specifications**

**A. Transistors**

All of the MOSFETs in this amplifier should be operated in strong inversion (as opposed to sub-threshold). Some of the transistors in the circuit can be chosen to be the smallest devices that can be made with the fabrication process used, but others will have to be designed to be larger; this might be done to adjust the value of a current source, for example, or to maximize the gain of a stage. In the listing below the properties of the minimum size devices are listed first and then the scaling rules for designing larger devices are given.

1. **npn Bipolar Transistors** -- The npn transistors are vertical structures that have the following large-signal and small-signal (hybrid-π) parameters

   a) **Minimum size devices**
   
   i) $\beta_F = 200$
   
   ii) $I_C = 100 \mu A$ when $V_{BE} = 0.6 \, V$ (i.e. $I_{ES} = 10^{-14} \, A$)
   $V_{CE,sat} = 0.2 \, V$
   
   iii) $g_m = q|I_C|/kT$, $g_n = g_m/\beta_F$
   $g_o = |I_C|/|V_A|$ with $|V_A| = 50V$
   
   iv) Operating range: $1.0 \, \mu A \leq I_C \leq 3 \, mA$

   b) **Scaled devices** -- You may increase the base-emitter junction area by up to a factor of 25 times. Increasing the base-emitter junction area, $A_{BE}$, by a factor of $\gamma$, increases the current limits on the operating range by the same factor. The emitter-base diode saturation current in the Ebers-Moll model, $I_{ES}$, increases by the same factor, $\gamma$; so too does $I_{CS}$. No other static model parameters change.

2. **pnp Bipolar Transistors** -- The pnp transistors are lateral structures that have the following large-signal and small-signal (hybrid-π) parameters

   a) **Minimum size devices**
   
   i) $\beta_F = 100$
   
   ii) $I_C = -100 \, \mu A$ when $V_{BE} = -0.6 \, V$ (i.e. $I_{ES} = 10^{-14} \, A$)
   $V_{CE,sat} = -0.2 \, V$
   
   iii) $g_m = q|I_C|/kT$, $g_n = g_m/\beta_F$
   $g_o = |I_C|/|V_A|$ with $|V_A| = 50V$
   
   iv) Operating range: $0.5 \, \mu A \leq I_C \leq 1.5 \, mA$

   b) **Scaled devices** -- You may increase the base-emitter junction area by up to a factor of 25 times. Increasing the base-emitter junction area, $A_{BE}$, by a factor of $\gamma$, increases the current limits on the operating range by the same factor. The emitter-base diode saturation current in the Ebers-Moll model, $I_{ES}$, increases by the same factor, $\gamma$; so too does $I_{CS}$. No other static model parameters change.
3. **n-channel MOSFET’s** -- The n-channel MOSFET’s are enhancement-mode devices with the following large and small-signal parameters.

   **a) Minimum size devices** \( (W = W_{\text{min}}, L = L_{\text{min}}) \)
   
   i) \( K = 5.0 \text{ mA/V}^2 \quad \alpha = 1 \)
   
   ii) \( V_T = +0.4 \text{ V} \)
   
   iii) \( g_m = K(V_{GS} - V_T) = (2KI_D)^{1/2} = 2I_D/(V_{GS} - V_T) \)
   
   \( g_o = \lambda I_D = I_D/|V_A| \) with \( |V_A| = 10 \text{ V} \)
   
   iv) Operating range: \( (V_{GS} - V_T) \geq 0.2 \text{ V} \)

   **b) Scaled devices** -- The width of the gate (and channel), \( W \), can be as large as \( 50 W_{\text{min}} \). The gate length should be \( L_{\text{min}} \) for \( Q_9 \) and \( Q_{10} \); for all other n-channel MOSFETs it can be long as \( 4 L_{\text{min}} \); however, the lengths of \( Q_{11} \), \( Q_{12} \), and \( Q_{22} \) should be the same. The magnitude of the Early voltage increases linearly with \( L \).

4. **p-channel MOSFET’s** -- The p-channel MOSFET’s are enhancement-mode devices with the following large and small-signal parameters.

   **a) Minimum size devices** \( (W = W_{\text{min}}, L = L_{\text{min}}) \)
   
   i) \( K = 2.5 \text{ mA/V}^2 \quad \alpha = 1 \)
   
   ii) \( V_T = -0.4 \text{ V} \)
   
   iii) \( g_m = K(V_{SG} - |V_T|) = (2KI_D)^{1/2} = 2I_D/(V_{SG} - |V_T|) \)
   
   \( g_o = \lambda |I_D| = I_D/|V_A| \) with \( |V_A| = 20 \text{ V} \)
   
   iv) Operating range: \( (V_{SG} - |V_T|) \geq 0.2 \text{ V} \)

   **b) Scaled devices** -- The width of the gate (and channel), \( W \), can be as large as \( 50 W_{\text{min}} \). The gate length should be \( L_{\text{min}} \) for \( Q_{13} \) and \( Q_{14} \); for all other p-channel MOSFETs it can be long as \( 4 L_{\text{min}} \); however, the lengths of \( Q_{14} \), \( Q_{15} \), and \( Q_{22} \) should be the same. The magnitude of the Early voltage increases linearly with \( L \).

**B. Power Supplies**

The power supplies are ideal voltage sources with fixed values of 1.5 V and -1.5 V relative to ground.

**V. Discussion of the Circuit**

You should first look at the circuit carefully and identify its various pieces. Initially the circuit looks very complicated but if you break it into its component parts and understand what each does and how they interact, you will find that the amplifier is actually much less formidable.

Begin by identifying the biasing circuitry and the current sources, in this case three p-channel MOSFETs \( (Q_1, Q_{12}, \text{and } Q_{19}) \), three n-channel MOSFETs \( (Q_4, Q_{11}, \text{and } Q_{22}) \), and two MOSFETs \( (Q_2 \text{ and } Q_3) \) that you can choose to make either n- or p-channel. (You must also specify where the gates and substrates of \( Q_2 \) and \( Q_3 \) are connected.)
The chain formed by \(Q_1, Q_2, Q_3,\) and \(Q_4\) determines the voltages at points A and B, which are used to establish the gate-to-source voltages of the transistors functioning as current sources, \(Q_{11}, Q_{12}, Q_{19},\) and \(Q_{22}.\) Specifically, \(Q_{11}\) functions as a current source that directly biases the first stage (transistors \(Q_5, Q_6, Q_7, Q_8,\) and \(Q_{10}.\)) \(Q_{12}\) functions as a current source that directly biases the second stage (transistors \(Q_{13}, Q_{14}, Q_{15}, Q_{16}, Q_{17},\) and \(Q_{18}.\)) Transistors \(Q_{19}\) and \(Q_{22}\) function as current sources that bias \(Q_{20}\) and \(Q_{21},\) the active transistors in the pnp and npn BJT emitter follower stages, respectively; they also indirectly bias \(Q_{23}\) and \(Q_{24}.\)

Once you see which transistors are involved in current source biasing you can mentally replace them with current sources, as we will do in Figure 2, and ignore those devices initially, and until you have decided what levels of bias current you need.

Move on next to look at the amplifier stages, starting with the input stage, \(Q_9\) and \(Q_{10}.\) This stage is an n-channel MOSFET source-coupled pair differential gain stage, loaded with an active load called the Lee Load. Incrementally the Lee Load looks like a very large resistor for differential-mode inputs, and like a very much smaller resistor for common-mode inputs. Thus the difference-mode voltage gain is very large and the common-mode voltage gain is much less than one (i.e., it is not a gain, but an attenuation). Using the Lee Load thus results in a gain stage with a large common-mode rejection ratio.

The second stage is another source-coupled pair differential gain stage, this time made with p-channel MOSFETs and loaded with another active load, a MOSFET current mirror load. p-channel MOSFETs are used for the active transistors in this second gain stage to get a wider voltage swing following the n-channel MOSFET first gain stage. Using a current mirror does two things:

\[\text{Figure 2} - \text{A simplified schematic of the design problem circuit drawing attention to some of the functional units of the circuit. There are four stages in this amplifier: From left to right, we find that Stage 1 is an n-MOS source-coupled pair gain stage with a p-MOS Lee Load; Stage 2 is a p-MOS source-coupled pair gain stage with an n-MOS current mirror load; Stage 3 is a complementary pair of emitter-follower buffer stages; and Stage 4 is a bipolar push-pull output stage (this is essentially another emitter-follower stage).}\]

\(^*\) Named after Professor Tom Lee of Stanford (a former 6.012 student) who invented it, though not in 6.012.
First, it is an active load that effectively applies the output of $Q_{13}$ to the gate of $Q_{16}$, so that the output due to the difference-mode signal input to $Q_{13}$ is added to the output due to the difference-mode signal input to $Q_{14}$. Doing this converts the output from a double-ended (or differential) output to a single-ended output, and does so in such a manner that we obtain an additional factor of two in gain. (This is explained in Section 12.4, pages 392-395 in the Course Text.)

Second, the output resistance of the current mirror load looks different for common-mode and difference-mode signals, just as was the case with the Lee Load. As a consequence the difference-mode gain of this stage is large, while at the same time, the common mode gain of this stage is small.

The two transistors $Q_{17}$ and $Q_{18}$ are connected as diodes and are included to increase quiescent voltage of the drains of $Q_{13}$ and $Q_{14}$ and thereby reduce the DC offset voltage (see below). These transistors ($Q_{17}$ and $Q_{18}$) could have been connected in a "cascode" connection to increase the output resistance of the current mirror load, but there is little advantage to doing this in this circuit since a bipolar output stage is used. (Using a diode connection also simplifies the design problem.)

The output of the second stage is taken from the node joining the drain of $Q_{14}$ and the drain of $Q_{16}$. This node is what is called a “high impedance” node. Ideally the voltage on this node would match that on the node joining the drains of $Q_{13}$ and $Q_{15}$ and the voltage on this latter node is known because it is connected to the gates of $Q_{15}$ and $Q_{16}$.

The goal is to make the quiescent voltage on the drain of $Q_{13}$ as close to zero as possible without limiting the output voltage swing, but it is not possible, nor is it necessary, to make it high enough to itself yield $V_{OUT} = 0 \text{ V}$. In practice, the quiescent value of the voltage on the drain of $Q_{14}$ is very sensitive to differences in the transistors and process variations, and as a practical matter it cannot be predicted with certainty. This is a very common situation in high gain differential amplifiers and it is dealt with by using the amplifier with feedback that stabilizes the quiescent output voltage very near to zero Volts. The practical consequence for your analysis is that you can assume that the quiescent output voltage is zero volts. You should then calculate how much of a differential bias voltage is needed at the input of your design to make $V_{OUT} \approx 0 \text{ V}$ assuming perfect matching (this will be discussed in class).

The third “stage is a complementary pair of emitter-follower stages, one that uses a pnp BJT ($Q_{20}$) and the other that uses an npn BJT ($Q_{21}$). These followers are coupled to the fourth and final stage, which is a complementary output stage called a push-pull, or totem-pole, stage. This is basically an emitter-follower stage in which an npn bipolar transistor ($Q_{23}$ in this circuit) drives the load (i.e., supplies current to the load resistor) when the output voltage goes above zero, and a pnp bipolar transistor ($Q_{24}$) drives the load when the voltage goes negative.

With zero input voltage, all four transistors, $Q_{20}$, $Q_{21}$, $Q_{23}$, and $Q_{24}$, are equally on, $v_{BE20} + v_{BE23} = 0$, $v_{BE21} + v_{BE24} = 0$, and $v_{OUT} = 0$. However, as the output signal goes positive the pnp transistors are turned off ($v_{EB20}$ and $v_{EB24}$ decrease) and the npn transistors turn on more strongly ($v_{EB21}$ and $v_{EB23}$ decrease) supplying current
to the load through \( Q_{23} \) and making \( v_{\text{OUT}} \) positive. When the output goes negative, the opposite happens and the pnp transistor, \( Q_{24} \), turns on strongly drawing current through the load and making \( v_{\text{OUT}} \) negative.

Taken together the last two stages give the amplifier a low output resistance and provide a buffer between the 50 Ohm load and the high gain second stage. (See Section 11.3.4, and especially the discussion on Page 345, in the Course Text. This is a different push-pull design than that in the text, but the basic idea is the same.) The interactions between the output stages and the second gain stage are particularly important to consider: First, \( Q_{20} \) and \( Q_{21} \) should be sized and biased so that there is no bias current drawn from the second stage. You will find, in fact, that the relative sizes of all of the bipolar transistors (\( Q_{23r} \), \( Q_{21r} \), \( Q_{23} \), and \( Q_{24} \)) are important to consider when designing the biasing. Second, the input resistance of the two complementary emitter follower stages (\( Q_{20} \) and \( Q_{21} \)) loads the current mirror gain stage and plays an important role in limiting the gain of that stage. Third, the output resistance of the amplifier is limited in large part by the output resistance of the second gain stage. The bias currents set by \( Q_{19} \) and \( Q_{22} \) also play an important role in setting the output resistance and you will find that there is a clear trade-off between output resistance and quiescent power dissipation. All told, the output stages are perhaps the most interesting part of the circuit, as will become more clear as the design problem circuit is discussed in lecture, recitation, and tutorials.

VI. **Starting your Analysis**

As pointed out earlier, one of the first things to do is to identify the various sub-circuits in the full circuit, i.e., the various gain stages, the biasing circuitry, etc. Then look at each piece individually and understand what it can do and what constraints are placed upon it. Look at each gain stage, for example, and write an expression for its gain. Try to get a relationship that depends on the bias level and device parameters, and then on any bounds on the dimensions of the devices, and on any limitations on the operating currents and/or voltages of the devices. We know in general, for example, that MOSFET gain stages loaded with non-linear loads formed from transistors biased in their constant current regions (i.e., saturation in the case MOSFETs operated in strong inversion) tend to have higher gain when biased at low levels of drain current, that is, with small values of \( (|V_{GS}| - |V_T|) \). Since there is a minimum value this quantity can have, it will be useful to try to express the gain of the current mirror gain stage in terms of \( (|V_{GS}| - |V_T|)_{\text{min}} \), and find what the maximum gain for the stage can be. Then you can begin to understand how you must size and bias the stage to achieve that gain (or as near to it as possible).

To help you get started understanding the incremental behavior of the amplifier, partial small signal linear equivalent circuits for the amplifier with difference- and common-mode inputs respectively are shown in Figure 3a and 3b. You do not need to work out the effective resistances of the Lee and Current Mirror loads, but rather you can use the gain expressions you will be given in class. However, do make sure that you have all the factors of two correctly accounted for, etc. (i.e., don't apply the equations your are given blindly).

You should also spend some time understanding the output stages as they are the most complex part of the design. Begin with the output resistance and how it is related to the bias level of the last follower stage. This will give you a
good idea of how that stage will have to be biased. Understanding how the bias of the last stage is established is very important. Also study the resistance seen looking into the follower stages from the output of the current mirror second gain stage, because it will impact the gain of that stage. To analyze the final stage you can assume that both of the transistors are active for your incremental modeling, whereas for your large signal analysis of the maximum output voltage swing, only one of these transistors will be on at a time. All of these points will be discussed in class.

The biasing circuitry, particularly the reference stack of $Q_1$ thru $Q_4$, can be viewed as a separate issue in terms of understanding how it operates. Once you do this you can understand how to size the various transistors to achieve the bias

![Diagram](image.png)

**Figure 3 -** Partial linear equivalent circuits for the design problem circuit for difference-mode and common-mode inputs. The transistors have to be replaced by their linear equivalent circuits to get the complete linear equivalent circuit of the amplifier, and the factor of 2 enhancement from the current mirror also has to taken into account, but these abstractions help one gain insight.
levels you need based on your understanding and analysis of the amplifier proper. Of course, there may be limitations placed on the bias levels you can achieve that force you to adjust your designs for the amplifier stages, so look the design of Q₁ thru Q₄ stack early in your design. The but by that point your understanding of the circuits should be such that making any such adjustments is not a major calamity; a major pain maybe, but no cause for panic.

A second set of things you should do early in your design process is to look through the design specifications and understand upon what each depends. As you develop an understanding of the circuit, you can write expressions for the various quantities specified (i.e., voltage gains, input and output resistances, etc.). Look also at the device specifications, and at what you can and cannot do in terms of adjusting device sizes.

Once you begin to understand the pieces and the specifications, make some initial design choices and see what you get. You may find that some parts work just fine, while others require major reworking. It may take several iterations to meet all of the specifications, but the more you understand the pieces and their interactions, and understand the implications for the circuit of the constraints placed on the sizes and operating ranges of the devices, the more quickly you can get to the answer and the less of a random walk your effort will seem.

Various aspects of the design problem will be discussed in lectures and the slides used in those discussions will be collected together and posted on Stellar for your reference.

VII. Enhancements to the Circuit

You are, of course, encouraged to design your circuit to surpass the design performance specifications, particularly the gain specs, by as much as possible. In addition, you are encouraged to think about (and discuss in your write up) ways that the circuit could be improved beyond the present design, as well as why certain choices were not made in the design. For example, You might want to consider using MOSFETs in the output stages, and seeing whether they offer performance advantages. You could then also consider using a cascode in the second gain stage, which would significantly increase the open circuit gain of that stage. This would also considerably increase the output resistance of the current mirror stage, but with MOSFET followers this is not the issue it is with BJT followers.

VIII. Go for It

What I’d do if I were you: Read this document through and get a feel for scope of things and especially why biasing at a small (V_{GS}-V_T) is good. Then start on the left with the design of the Q₁ to Q₄ bias reference tree. Then look at the two gain stages in turn. The Lee Load stage gain is easiest, then go on to the gain of the Current Mirror Load stage. It's gain ultimately depends on the design of the last two stages, so once you see that and figure out how it comes about, set the final design of the second stage aside for awhile and look at designing the follower stages. They are the most complex. First figure out the constraints on their biasing, i.e. on I_{BIAS3} and I_{BIAS4} (how they must be related; not final their values yet). Then look at the output resistance spec and what it says about the biasing of these stages. Next look at the input resistance to these stages, and to their voltage gains. With all of this, you can finalize the design of the second gain stage and the follower stages...and go to bed.