6.012 - Microelectronic Devices and Circuits
Lecture 21 - **Diff-Amp Anal. II: Output Stages** - Outline

- **Announcements**
  - DP: Get help before next weekend. It's due Friday, May 6
  - On Stellar: Write-up on the Cascode connection posted under Lec. 22. Lee Load and Current Mirror Load write-ups posted under Lec. 20. Design problem slides collected together under DP Header

- **Review - Non-linear and Active Loads**
  - Maximum gain: $A_{v,max} \propto \frac{V_{A,eff}}{(V_{GS}-V_T)_{min}}$ for MOS; $\propto \frac{V_{A,eff}}{V_{thermal}}$ for BJT
  - Lee Load, Current Mirror: foils on analysis of CM in DP

- **Specialty Stages - useful transistor pairings, first round**
  - Source-coupled pairs, Current mirror
  - Push-pull or Totem Pole output stages
  - Cascode, Darlington, EF-CB Pair

- **Performance metrics - continuing down the list**
  - Output resistance: Driving a load
  - DC off-set on output: High impedance nodes; feedback connections
  - Power dissipation: Add up currents from voltage supplies
Achieving the maximum gain: Comparing linear resistors, current sources, and active loads

<table>
<thead>
<tr>
<th>Maximum Gains</th>
<th>MOSFET (SI) (w. and w.o. velocity sat.)</th>
<th>Bipolar-like (Sub-V&lt;sub&gt;T&lt;/sub&gt; MOS and BJT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linear resistor loads</td>
<td>$\leq \frac{2 \alpha V_{DD}}{v_{GS} - V_T}_{\text{min}}$</td>
<td>$\leq \frac{\alpha V_{DD}}{n V_t}$</td>
</tr>
<tr>
<td>Current source loads</td>
<td>$\leq \frac{2 V_{A,eff}}{v_{GS} - V_T}_{\text{min}}$</td>
<td>$\leq \frac{V_{A,eff}}{n V_t}$</td>
</tr>
<tr>
<td>Active loads</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Difference mode</td>
<td>$\propto \frac{2 V_{A,eff}}{v_{GS} - V_T}_{\text{min}}$</td>
<td>$\propto \frac{V_{A,eff}}{n V_t}$</td>
</tr>
<tr>
<td>Common mode</td>
<td>$\propto \frac{2 V_{A,bias}}{v_{GS} - V_T}_{\text{min}}$</td>
<td>$\propto \frac{n V_t}{V_{A,bias}}$</td>
</tr>
</tbody>
</table>

Observations/Comments:
- Non-linear (current source) loads typically yield much higher gain than linear resistors, i.e. $V_{A,eff} >> \alpha V_{DD}$ ($\equiv [I_{D}R_{SL}]_{\text{max}}$ used in Lec. 20)
- The bias point is not as important to BJT-type stage gain.
- An SI MOSFET should be biased just above threshold for highest gain.
- For active loads what increases $A_{vd}$ decreases $A_{vc}$.
- Making L larger increases $V_A$ proportionately, but at the cost of speed.
Achieving the maximum gain: \((V_{GS}-V_{T})_{\text{min}} = ?\)

For SI-MOSFETs, maximizing the voltage gain \((A_{v} \text{ or } A_{vd})\) requires minimizing \((V_{GS}-V_{T})\). What is the limit?

Strong inversion:

\[
\left| \frac{A_v}{V_{A,\text{eff}}} \right| = \frac{2}{(V_{GS} - V_{T})}
\]

Sub-threshold:

\[
\left| \frac{A_v}{V_{A,\text{eff}}} \right| = \frac{1}{n \cdot V_{t}}
\]

\(A_{v}/V_{A,\text{eff}}\) is a smooth curve, so clearly \((V_{GS}-V_{T})_{\text{min}} >> 2nV_{t}\).

Note: \(n = 1.25\) was assumed.
What if we want an active load and yet stay differential?

**Active Loads** - The Lee load

A load for a fully-differential stage that looks like a large resistance in difference-mode and small resistance in common-mode.

The conventional schematic is drawn here, but the coupling of the load and what is happening is made clearer by redrawing the circuit (next slide.)
Active Loads - The Lee load. cont.

Drawn as on the right we see that the load MOSFETs on each side are driven by both outputs. The result is different if the two outputs are equal and opposite (diff-mode operation) or if they are equal (common-mode).

The next few slides give the results for each mode.

Drawn to highlight cross-coupling and demonstrate symmetry.
The Lee load: analysis for difference-mode inputs

**LEHC: difference-mode**

\[
\frac{v_id}{2} = v_{gs5} \\
\frac{g_{m5}v_id}{2} g_{o5} g_{m1}v_{od}/2 - g_{m3}v_{od}/2 g_{o3} v_{od}/2 g_{el}\\n\]

\[ g_{oLLd} \]
The Lee load: analysis for difference-mode inputs, cont

Note: In D.P., the outputs go to MOSFET gates so $g_{el} = 0$. 

$$A_{vd} = \frac{V_{od}}{V_{id}} = \frac{-g_{m5}}{g_{o5} + 2g_{o1} + g_{e1}}$$

$$g_{oLLd} = 2g_{o1}$$
The Lee load: analysis for common-mode inputs

LEHC: common-mode

\[ g_{oLLc} \]

\[ V_{gs5} \]

\[ g_{m5} V_{gs5} \]

\[ g_{o5} \]

\[ V_{ic} \]

\[ g_{ob}/2 \]

\[ g_{m1} V_{oc} \]

\[ g_{o1} \]

\[ g_{m3} V_{oc} \]

\[ g_{o3} \]

\[ V_{oc} \]

\[ g_{el} \]
The Lee load: analysis for common-mode inputs, cont

**LEHC: common-mode**

\[ g_{oLLc} = 2(g_{m1} + g_{o1}) \approx 2g_{m1} \]

\[ A_{vc} = \frac{v_{oc}}{v_{ic}} = \frac{-g_{ob}}{2[2(g_{m1} + g_{o1}) + g_{el}]} \approx -\frac{g_{ob}}{4g_{m1}} \]

Note: In D.P., the outputs go to MOSFET gates so \( g_{el} = 0 \).

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The Lee load: applying these results to the Design Problem

\[ Q_n \rightarrow Q_{n+4}, \quad g_{el} = 0, \quad I_{\text{BIAS}} = I_{\text{BIAS1}}, \quad g_{ob} \rightarrow g_{o11} \]

**Difference-mode Gain**

\[
A_{vd} = \frac{v_{od}}{v_{id}} = \frac{-g_{m9}}{(g_{o9} + 2g_{o5})} = -\frac{2(I_{\text{BIAS1}}/2)}{(V_{GS9} - V_T)} = -\frac{2}{(V_{GS9} - V_T)} \left( \frac{I_{\text{BIAS1}}/2}{V_{A9}} + \frac{2I_{\text{BIAS1}}/4}{V_{A5}} \right)
\]

**Common-mode Gain**

\[
A_{vc} = \frac{v_{oc}}{v_{ic}} = \frac{-\left(g_{o11}/2\right)}{\left[2\left(g_{m5} + g_{o5}\right)\right]} \approx -\frac{g_{o11}}{4g_{m5}} = -\frac{I_{\text{BIAS1}}}{V_{A11}} = -\frac{2}{2V_{A11}} \left( \frac{I_{\text{BIAS1}}/4}{V_{SG5} - |V_T|} \right)
\]

**Overall**

\[
\begin{align*}
\frac{v_{out1,s1} - v_{out2,s1}}{2} & = -\frac{2}{(V_{GS9} - V_T)} \frac{V_{A5}V_{A9}}{V_{A9} + V_{A5}} \left( v_{in1} - v_{in2} \right) \\
\frac{v_{out1,s1} + v_{out2,s1}}{2} & = -\frac{\left( V_{SG5} - |V_T| \right)}{2V_{A11}} \left( v_{in1} + v_{in2} \right)
\end{align*}
\]
Active Loads: The current mirror load

Large differential-mode gain, small common-mode gain. Also provides high gain conversion from double-ended to single-ended output.

The circuit is no longer symmetrical, so half-circuit techniques can not be applied. The full analysis is found in the course text. We find:

\[
v_{out,d} = \frac{2g_m}{g_{o2} + g_{o4} + g_{el}} \cdot \frac{v_{id}}{2}
\]
Active Loads: The current mirror load, cont.

Common-mode inputs

\[ v_{out,c} = \frac{g_{ob}}{2g_{m2}} v_{ic} \]

With both inputs:

\[ v_{out} = \frac{2g_{m3}}{g_{o2} + g_{o4} + g_{el}} \left( \frac{v_{in1} - v_{in2}}{2} \right) - \frac{g_{ob}}{2g_{m2}} \left( \frac{v_{in1} + v_{in2}}{2} \right) \]

Note: In D.P. the output goes to the gate of a BJT; \( g_{el} \) matters.
Current mirror load: application to the Design Problem

\[ Q_1 \rightarrow Q_{15}, \; Q_2 \rightarrow Q_{16}, \; Q_3 \rightarrow Q_{13}, \; Q_4 \rightarrow Q_{14}, \; g_{ob} \rightarrow g_{o12}, \; I_{BIAS} = I_{BIAS2} \]

**Total output** (Note: these inputs are stage inputs, not amplifier inputs)

\[
v_{out,s2} = \frac{2g_{m14}}{g_{o16} + g_{o14} + g_{el}} \left( \frac{v_{in1,s2} - v_{in2,s2}}{2} - \frac{g_{o12}}{g_{m16}} \left( \frac{v_{in1,s2} + v_{in2,s2}}{2} \right) \right)
\]

\[
= \frac{2 \left( \frac{I_{BIAS2}}{2} \right)}{\left( V_{SG14} - |V_T| \right)} \left( \frac{V_{A16}}{V_{A14}} + g_{el} \right) \left( \frac{v_{in1,s2} - v_{in2,s2}}{2} \right)
\]

\[
= \frac{4}{\left( V_{SG14} - |V_T| \right)} \left( \frac{1}{V_{A16}} + \frac{1}{V_{A14}} + \frac{2g_{el}}{I_{BIAS2}} \right) \left( v_{in1,s2} - v_{in2,s2} \right)
\]

\[
- \frac{V_{GS16} - V_T}{V_{A12}} \left( v_{in1,s2} + v_{in2,s2} \right)
\]

\[ * \text{ Note: } 2 \; g_{m2} \; \text{is replaced by } 2(1/g_{m16}+1/g_{m18})^{-1} =^* \; g_{m16}, \; \text{because in common-mode } Q_{16} \; \text{and } Q_{18} \; \text{are in series.} \]

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(** This equality is of course only valid if Q_{16} and Q_{18} are identical.)
Specialty Pairings: The Push-pull or Totem Pole Output

A stacked pair of complementary emitter- or source-followers

- Large input resistance
- Small output resistance
- Voltage gain near one
- Low quiescent power

npn or n-MOS follower

pnp or p-MOS follower

\[ V_+ \]

\[ Q_n \]

\[ \text{Vin} + V_{BE} \]

\[ \text{Vin} - V_{EB} \]

\[ V_0 \]

\[ R_L \]

\[ v_{out} \]

\[ V_- \]
Specialty pairings: Push-pull or Totem Pole Output Pairs

The limitations of using a simple follower stage* output:
- Using a single source follower as the output stage must be biased with a relatively large drain current to achieve a large output voltage swing, which in turn dissipates a lot of quiescent power.

* source follower or emitter follower
Specialty pairings: Push-pull or Totem Pole, cont.

- A p-MOS follower solves the negative swing problem, but has its own positive swing problem.

- The solution is to combine the two in a totem pole stack (and drive and bias them by the preceding stage).

Positive $v_{OUT}$ swing limited to $I_{BIAS}R_L$

As $Q$ turns off, $I_{BIAS}$ flows through load.

$v_{IN}$ goes positive

$Q$ turns off

$V_{OUT}$

$R_L$

$v_{IN}$

$-1.5\,V$

$+1.5\,V$

$Q_3$ and $Q_4$ bias $Q_2$ and $Q_5$. They also insure that $Q_5$ turns off as $Q_2$ turns on, and visa versa.

$Q_2$ supplies the load current for $v_{OUT} > 0$

$Q_5$ sinks the load current for $v_{OUT} < 0$
**Specialty pairings:** Push-pull or Totem Pole, cont.

**Comments/Observations:**

- The output resistance is largest around $v_{OUT} = 0$. Here both $Q_2$ and $Q_5$ are active and the output resistance is:
  
  $$r_{out} \approx \frac{1}{g_{m2} + g_{m5}}$$

- One must always make $K_2/K_3 = K_5/K_4$, and in the typical design $K_3 = K_4$, and $K_2 = K_5$. The bias current of $Q_2$ and $Q_5$ is set by $I_{BIAS}$:
  
  $$I_{D2} = |I_{D5}| = \left(\frac{K_2}{K_3}\right)I_{BIAS}$$

- $|v_{OUT}|$ vs $|v_{IN}|$ is fairly linear over a wide range (see right); $|v_{GS}|$ increases slowly with $|v_{IN}|$. 

![Diagram of push-pull or Totem Pole circuit](image)

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Specialty pairings: Push-pull or Totem Pole in Design Prob.

Comments/Observations:
- The D.P. output stage involves four emitter follower building blocks arranged as two parallel cascades of two emitter follower stages each.
- Driving the totem pole in this manner results in a much larger output voltage range than is obtained by using a single follower as was done in our earlier examples.

NOTE: Designing with this output requires paying special attention to the biasing, and calculating the input and output resistances.
Specialty pairings:  Push-pull or Totem Pole in D.P., cont.

Biasing the output stages:  getting the currents right

1. Constraint at input node:  \( I_{B21} = -I_{B20} \)
   Equivalently:  \( I_{E21}/(\beta_n + 1) = -I_{E20}/(\beta_p + 1) \)

2. Constraint at output node:  \( I_{E24} = -I_{E23} \)

3. Sum at emitter of \( Q_{20} \):
   \[
   I_{BIAS3} = I_{E20} - I_{E23}/(\beta_n + 1)
   \]
   \[
   = - (\beta_p + 1)I_{B20} - I_{E23}/(\beta_n + 1)
   \]
   \[
   = (\beta_p + 1) \left[ -I_{B20} + \frac{-I_{E23}}{(\beta_n + 1)(\beta_p + 1)} \right]
   \]

4. Sum at emitter of \( Q_{21} \):
   \[
   I_{BIAS4} = (\beta_n + 1)I_{21} + I_{E24}/(\beta_p + 1) = (\beta_n + 1) \left[ I_{B21} + \frac{I_{E24}}{(\beta_n + 1)(\beta_p + 1)} \right]
   \]

5. Combining everything:
   \[
   I_{BIAS2}/I_{BIAS3} = (\beta_p + 1)/(\beta_n + 1) \approx \beta_p/\beta_n
   \]

Lesson:  The bias currents are constrained.
Specialty pairings:  Push-pull or Totem Pole in D.P., cont.

Biasing the output stages: getting the voltages right

KVL constraint:

\[ V_{BE_{23}} + V_{EB_{24}} - V_{BE_{21}} - V_{EB_{20}} = 0 \]

Relating voltages to currents:

\[ V_{EB_{20}} = \left( \frac{kT}{q} \right) \ln \left[ I_{E_{20}}/\gamma_{20} I_{ESp} \right] \]
\[ V_{BE_{21}} = \left( \frac{kT}{q} \right) \ln \left[ -I_{E_{21}}/\gamma_{21} I_{ESn} \right] \]
\[ V_{BE_{23}} = \left( \frac{kT}{q} \right) \ln \left[ -I_{E_{23}}/\gamma_{23} I_{ESn} \right] \]
\[ V_{BE_{24}} = \left( \frac{kT}{q} \right) \ln \left[ I_{E_{24}}/\gamma_{24} I_{ESp} \right] \]

Combining everything, including the fact that \( I_{ESp} = I_{ESn} = I_{ES} \) and the results \( I_{E_{24}} = -I_{E_{23}} \) and \( I_{E_{20}}/\left( \beta_p + 1 \right) = -I_{E_{21}}/\left( \beta_n + 1 \right) \), yields:

\[ \frac{I_{E_{23}}}{I_{E_{21}}} = \sqrt{\frac{\left( \beta_p + 1 \right) \gamma_{23} \gamma_{24}}{\left( \beta_n + 1 \right) \gamma_{20} \gamma_{21}}} \]

Lesson: The BJT areas must be properly designed.
Specialty pairings:  Push-pull or Totem Pole in D.P., cont.

Reviewing the input and output resistances of an emitter follower:

\[ r_{in} = r_π + (β+1)(r_l \parallel r_o \parallel r_{Bias}) \]
\[ r_{in} \approx r_π + (β+1)r_l \]

\[ r_{out} = \frac{1}{[g_o + g_{Bias} + (β+1)/(r_π + r_t)]} \]
\[ r_{out} \approx (r_π + r_t)/(β+1) \]

The only two things you need to know:
- Looking in the resistance is multiplied by (β+1); looking back it is divided by (β+1).
Reviewing the voltage gain of an emitter follower:

\[
\begin{align*}
i_{\text{in}} &= i_b \\
v_{\text{in}} &= i_b r_\pi + (\beta + 1)i_b \left( r_l \parallel r_o \parallel r_{\text{Bias}} \right) \\
v_{\text{out}} &= \beta i_b \\
r_o \parallel r_{\text{Bias}}
\end{align*}
\]

\[
A_v = \frac{v_{\text{out}}}{v_{\text{in}}} = \frac{(\beta + 1)\left( r_l \parallel r_o \parallel r_{\text{Bias}} \right)}{r_\pi + (\beta + 1)\left( r_l \parallel r_o \parallel r_{\text{Bias}} \right)}
\]

\[
A_v \approx \frac{(\beta + 1) r_l}{r_\pi + (\beta + 1) r_l} = \frac{r_l}{r_\pi/(\beta + 1) + r_l} = \frac{r_l}{1/g_m + r_l}
\]

**Note:** The voltage gains of the third-stage emitter followers (Q_{17} and Q_{18}) will likely be very close to one, but that of the stage-four followers might be noticeably less than one.
Specialty pairings: Push-pull or Totem Pole in D.P., cont.

Operation: The npn follower supplies current when the input goes positive to push the output up, while the pnp follower sinks current when the input goes negative to pull the output down.

NOTE: Near \( v_{in} = 0 \) we have two paths in parallel, and this must be considered when finding \( r_{in} \) and \( r_{out} \).
Specialty pairings: Push-pull or Totem Pole in D.P., cont.
The input resistance of the output stages as seen by the Current Mirror

We will make the approximation that the two emitter-follower paths can be modeled as being in parallel for purposes of calculating the input resistance.

Note: $r_{in}$ is smallest around $v_{in} = 0$, so this is a worst-case estimate.
**Specialty pairings:** Push-pull or Totem Pole in D.P., cont.

The output resistance of the amplifier as seen by the 50 Ω load

We will make the approximation that the two emitter-follower paths can be modeled as being in parallel for purposes of calculating the output resistance.

\[ r_{\text{out}} \approx r_{\text{out1}} \parallel r_{\text{out2}} \]

Note: \( r_{\text{out}} \) is largest around \( v_{\text{out}} = 0 \), so this is a worst-case estimate.
**Push-Pull Stage Gain:** application to the Design Problem

\[
\begin{align*}
\frac{r_{\pi 23}}{(\beta_p + 1)} &= \frac{1}{g_{m23}} = \frac{1}{g_{m24}} = \frac{r_{\pi 24}}{(\beta_n + 1)} \\
\frac{r_{\pi 23}}{(\beta_p + 1)} &\parallel \frac{r_{\pi 24}}{(\beta_n + 1)} = \frac{1}{(g_{m23} + g_{m24})} = \frac{1}{2g_{m23}}
\end{align*}
\]

\[
A_{v,s4} = \frac{v_{out,s4}}{v_{in,s4}} \approx \frac{50}{50 + 1/2g_{m23}} = \frac{50}{50 + V_{th}/2I_{C23}}
\]

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Design Problem Stage Gains: Collected gain equations

(this slide will be fixed up more; watch for information in lecture)

Stage 1:
\[
\frac{v_{out, s1} - v_{out, s2}}{2} = -\frac{-g_m}{2} \left(\frac{v_{in1} - v_{in2}}{g_o + 2g_o} \right)
\]
\[
\frac{v_{out, s1} + v_{out, s2}}{2} = -\frac{g_{o1}}{4g_m} \left(\frac{v_{in1} + v_{in2}}{2} \right)
\]

Stage 2:
\[
v_{out, s2} = \frac{2g_m}{g_o + g_o + g_e} \left(\frac{v_{out, s1} - v_{out, s2}}{2} \right) - \frac{g_{o1}}{g_{m16}} \left(\frac{v_{out, s1} + v_{out, s2}}{2} \right)
\]

Stage 3:
\[
v_{out, s3} = v_{out, s2}
\]

Stage 4:
\[
v_{out, s4} = \frac{R_L}{1/2g_m + R_L} v_{out, s3}
\]
Specialty pairings: Push-pull or Totem Pole, cont.

Voltage gain via large signal analysis: (confirming/extending our LEC analysis)
- The gain and linearity of the push-pull output stage depend on the bias level of the totem pole. The gain is higher for with higher bias, but the power dissipation is also larger. To understand this more it is instructive to calculate the large signal transfer characteristic of the stage.

\[
\begin{align*}
\text{To calculate the large signal transfer characteristic of the bipolar totem pole we begin with } v_{\text{OUT}}: \\
v_{\text{OUT}} &= R_L \left(-i_{E23} - i_{E24}\right) \\
\text{The emitter currents depend on } (v_{\text{IN}} - v_{\text{OUT}}): \\
i_{E23} &= -I_{E23} e^{(v_{\text{IN}} - v_{\text{OUT}})/V_t}, \quad i_{E24} = I_{E24} e^{- (v_{\text{IN}} - v_{\text{OUT}})/V_t}
\end{align*}
\]

Putting this all together, and using \( I_{E24} = - I_{E23} \), we have:

\[
\begin{align*}
v_{\text{OUT}} &= R_L I_{E23} \left(e^{(v_{\text{IN}} - v_{\text{OUT}})/V_t} - e^{- (v_{\text{IN}} - v_{\text{OUT}})/V_t}\right) \\
&= 2 R_L I_{E23} \sinh\left((v_{\text{IN}} - v_{\text{OUT}})/V_t\right)
\end{align*}
\]

We can do a spread-sheet solution by picking a set of values for \( (v_{\text{IN}} - v_{\text{OUT}}) \), using the last equation to calculate the \( v_{\text{OUT}} \), using this \( v_{\text{OUT}} \) to calculate \( v_{\text{IN}} \), and finally plotting \( v_{\text{OUT}} \) vs \( v_{\text{IN}} \). The results are seen on the next slide.
Voltage gain, cont.:
- With a 50 Ω load and for several different bias levels we find:

The $A_v$ is lowest and $r_{out}$ is highest at the bias point (i.e., $V_{IN} = V_{OUT} = 0$). $r_{in}$ to the stage is also lowest there.

The gain and linearity are improved by increasing the bias current, but the cost is increased power dissipation.
DC off-set at the output of an Operational Amplifier:

DC off-set:
The node between $Q_{14}$ and $Q_{16}$ is a high impedance node whose quiescent voltage can only be determined by invoking symmetry.

The voltage on these two nodes is equal if there is no input, i.e. $v_{IN1} = v_{IN2} = 0$, and if the circuit is truly symmetrical/matched.

Note: The numbers used are hypothetical, and are not necessarily what they will be in a good design.

In any practical Op Amp, a very small differential input, $v_{IN1} - v_{IN2}$, is require to make the voltage on this node (and $V_{OUT}$) zero.

This is the high impedance node. Even if its voltage is designed to be zero, real-world asymmetries make it unpredictable.

What we get.**

What we want.

The voltage we need at this node to make $V_{OUT} = 0$.

** Assuming ideal matching.
DC off-set at the output of an Op Amp, cont:

DC off-set:

The transfer characteristic, \( v_{OUT} \) vs \( (v_{IN1} - v_{IN2}) \), will not in general go through the origin, i.e.,

\[ v_{OUT} = A_{vd} (v_{IN1} - v_{IN2}) + V_{OFFSET} \]

In the example in the figure, \( A_{vd} \) is \(-2 \times 10^6\), and \( V_{OFFSET} \) is 0.1 V.

In a practice, an Op Amp will be used in a feedback circuit like the example shown to the left, and the value of \( v_{OUT} \) with \( v_{IN} = 0 \) will be quite small. For this example (in which \( A_{vd} = -2 \times 10^6 \), and \( V_{OFFSET} = 0.1 \text{ V} \)) \( v_{OUT} \) is only 0.1 \( \mu \text{V} \).

In the D.P. you are asked for this value for your design.
Active loads - Lee load, Current mirror
Design Problem specific foils

Specialty stages - useful pairings
Source coupled pairs: MOSFET, BJT diff amps
Current Mirror: Another one we’ve seen already
Push-pull output: Emitter followers in vertical chain
Very low output resistance
Shared duties for positive and negative output swings
Cascode, Darlington, EF-CB pair: Still to come in Lecture 22

Diff Amp Metrics
Output resistance: View as followers in parallel; largest about zero.
Input resistance to follower stages: Ditto; smallest about zero.
Last stage voltage gain: Ditto; smallest about zero
DC off-set on output: Nulled out by slight differential mode input
Power consumption: Add up the current from the supplies