• Announcements
  HKN On-line Course Evaluation - Please do it! And feel good inside.
  Final - Monday, May 16, 9:00 am - noon, Walker Memorial Exam Room

• Review - Intrinsic high frequency limits of transistors
  **BJTs**: finite current gain at DC, otherwise the same
  **MOSFETs**: without velocity saturation
  with strong velocity saturation

• The IC Roadmap – Silicon going forward
  Review – CMOS Scaling Rules
  The evolution of size and performance with time

• Devices we have known - Where they are, and are going:
  **MOSFETs**: 5 nm Si, III-V high electron mobility transistors
  **BJTs**: InP based double heterojunction bipolar transistors
  **LEDs**: white lighting; laser diodes
  **Solar cells**: multi-junction, multi-material concentrator cells
Intrinsic performance - the best we can do

We've focused on $\omega_{HI}$, the upper limit of mid-band, but even when $\omega > \omega_{HI}$ the $|A_v| > 1$, and the circuit is useful. For example, for the common source stage we had

$$A_v(j\omega) = \frac{-g_t(g_m - j\omega C_{gd})}{\left\{(j\omega)^2 C_{gs} C_{gd} + j\omega \left[ (g_l + g_o)C_{gs} + (g_l + g_o + g_t + g_m)C_{gd} \right] + (g_l + g_o)g_t \right\}}$$

A Bode plot of $A_v$ is shown to the right:

When we look for a metric to compare the ultimate performance limits of transistors, we make note of this and ask how high can a device in isolation have provide voltage or current gain?
The magnitude of $\beta_{sc}$ decreases above $\omega_b$, but it is still greater than one initially:

$$|\beta_{sc}(j\omega)| = \sqrt{\frac{g_m^2 + \omega^2 C^2_{\mu}}{g^2_{\pi} + \omega^2 (C_{\pi} + C_{\mu})^2}}$$

The transistor is useful until $|\beta_{sc}|$ is less than one. The frequency at which this occurs is called $\omega_t$. Setting $= 1$ and solving for $\omega_t$ yields:

$$\omega_t = \sqrt{\frac{(g^2_{\pi} + g^2_m)}{\left[(C_{\pi} + C_{\mu})^2 - C^2_{\mu}\right]}} \approx \frac{g_m}{(C_{\pi} + C_{\mu})}$$
BJT short-circuit current gain, $\beta_{sc}(j\omega)$, cont.

Can we bias to maximize $\omega_t$?

$$\omega_t \approx \frac{g_m}{\left( C_\pi + C_\mu \right)} = \frac{qI_C}{kT} \left( \frac{qI_C}{kT} \tau_b + C_{eb,dp} + C_{cb,dp} \right)$$

**Maximize $I_C$.**

Used $C_\pi = g_m \tau_b + C_{eb,dp}$

In the limit of large $I_C$:

$$\lim_{I_C \to \infty} \omega_t \approx \frac{1}{\tau_b} = \frac{2D_{\text{min,}B}}{W_B^2} = \frac{2\mu_{\text{min,}B} V_{\text{thermal}}}{W_B^2}$$

**Lessons:** Bias at large $I_C$; make $W_B$ small, use npn.
Intrinsic $\omega_{Hi}$'s for MOSFETs - short-circuit current gain, cont.

The magnitude of $\beta_{sc}$ decreases with $\omega$, but it is still greater than one for a wide range of frequencies.

$$|\beta_{sc}(j\omega)| = \left| \frac{g_m^2 + \omega^2 C_{gd}^2}{\sqrt{\omega^2 (C_{gs} + C_{gd})^2}} \right|$$

The transistor is useful until $|\beta_{sc}|$ is less than one. The frequency at which this occurs is called $\omega_t$. Setting $= 1$ and solving for $\omega_t$ yields:

$$\omega_t = \sqrt{\frac{g_m^2}{\left[ (C_{gs} + C_{gd})^2 - C_{gd}^2 \right]}} \approx \frac{g_m}{C_{gs} + C_{gd}}$$
MOSFET short-circuit current gain, \( \beta_{sc}(j\omega) \), cont.

Can we bias to maximize \( \omega_t \)?

\[
\omega_t \text{(MOSFET)} = \frac{g_m}{(C_{gs} + C_{gd})} \approx \frac{g_m}{C_{gs}}
\]

\[
= \frac{W}{L} \mu_{Ch} C^*_{ox} |V_{GS} - V_T|
\]

\[
= \frac{2}{3} \frac{W}{L} C^*_{ox}
\]

\[
= \frac{3}{2} \frac{\mu_{Ch} |V_{GS} - V_T|}{L^2}
\]

Maximize \( V_{GS} \).

What is the ultimate limit?

\[
\omega_t \text{(MOSFET)} = \frac{3}{2} \frac{\mu_{Ch} |V_{GS} - V_T|}{L^2} = \frac{3}{2L} \frac{\mu_{Ch} |V_{DS}|}{L} = \frac{3}{2L} \frac{\mu_{Ch} E_{Ch}}{L} = \frac{3}{2} \frac{s_{Ch}}{L} = \frac{1}{\tau_{Ch}}
\]

Lessons: Bias at large \( I_D \); make \( L \) small, use n-channel.

Can we bias to maximize \( \omega_t \)?

Maximize \( V_{GS} \).

Channel transit time!
Intrinsic $\omega_T$ for MOSFETs – with full velocity saturation

What about the intrinsic $\omega_{HI}$ of a MOSFET operating with full velocity saturation?

The basic result is unchanged; we still have:

$$\omega_t = \sqrt{\frac{g_m^2}{\left(C_{gs} + C_{gd}\right)^2 - C_{gd}^2}} \approx \frac{g_m}{C_{gs} + C_{gd}} \approx \frac{g_m}{C_{gs}}$$

However, now $g_m$ is different:

$$g_m = W s_{sat} C_{ox}^*$$

With this we have:

$$\omega_t \approx \frac{g_m}{C_{gs}} = \frac{W s_{sat} C_{ox}^*}{W LC_{ox}^*} = \frac{s_{sat}}{L} = \frac{1}{\tau_{Ch}}$$

In the case where velocity saturation dominates, we once again find that it is the channel transit time that is the ultimate limit.
An aside: looking back at CMOS gate delays

**CMOS:** switching speed; minimum cycle time (from Lec. 14)

**Gate delay/minimum cycle time:**

For MOSFETs operating in strong inversion, no velocity saturation:

\[ \tau_{\text{MinCycle}} = \frac{12nL_{\text{min}}^2 V_{DD}}{\mu_e [V_{DD} - V_{Tn}]^2} \]

Comparing this to the channel transit time:

\[ \tau_{\text{ChTransit}} = \frac{L_{\text{min}}}{\bar{s}_{e,Ch}} = \frac{L_{\text{min}}}{\mu_e E_{Ch}} = \frac{L_{\text{min}}}{\mu_e (V_{DD} - V_{Tn})/L_{\text{min}}} \]

We found cycle time is a multiple of the transit time:

\[ \tau_{\text{MinCycle}} = \frac{12nV_{DD}}{(V_{DD} - V_{Tn})} \tau_{\text{ChannelTransit}} = n' \tau_{\text{ChannelTransit}} \]

When velocity saturation dominated, we found the same thing:

\[ \tau_{\text{MinCycle}} \propto \frac{L_{\text{min}} V_{DD}}{s_{sat} [V_{DD} - V_{Tn}]} = n' \tau_{\text{ChanTransit}} \quad \text{where} \quad \tau_{\text{ChanTransit}} = \frac{L}{s_{sat}} \]
**CMOS:** design for high speed

**Maximum data rate**

Proportional to $1/\tau_{\text{Min Cycle}}$

\[
\tau_{\text{Min Cycle}} = \tau_{\text{Ch arg e}} + \tau_{\text{Disch arg e}} = \frac{12nL_{\text{min}}^2 V_{\text{DD}}}{\mu_e [V_{\text{DD}} - V_{Tn}]^2}
\]

Implies we should reduce $L_{\text{min}}$ and increase $V_{\text{DD}}$.

**Note:** As we reduce $L_{\text{min}}$ we must also reduce $t_{\text{ox}}$, but $t_{\text{ox}}$ doesn't enter directly in $f_{\text{max}}$ so it doesn't impact us here.

**Power density at maximum data rate**

Assume that the area per inverter is proportional to $W_{\text{min}}L_{\text{min}}$

\[
P_D\text{ dyn @ }f_{\text{max}} \propto \frac{P_{\text{dyn @ }f_{\text{max}}}}{W_{\text{min}}L_{\text{min}}} = \frac{\mu_e \varepsilon_{\text{ox}} V_{\text{DD}} [V_{\text{DD}} - V_{Tn}]^2}{t_{\text{ox}} L_{\text{min}}^2}
\]

Shows us that $PD$ increases very quickly as we reduce $L_{\text{min}}$ unless we also reduce $V_{\text{DD}}$ (which will also reduce $f_{\text{max}}$).

**Note:** Now $t_{\text{ox}}$ does appear in the expression, so the rate of increase with decreasing $L_{\text{min}}$ is even greater because $t_{\text{ox}}$ must be reduced along with $L$ to stay in the gradual channel regime.

How do we make $f_{\text{max}}$ larger without melting the silicon? **Constant field scaling.**
Scaling Rules - constant E-field scaling

**Observation:**
Reducing dimensions alone won't work.
Reduce voltage in concert (constant E-field scaling)

**Scaling dimensions and voltages by 1/s:**

\[ L_{\text{min}} \rightarrow L_{\text{min}}/s \quad W \rightarrow W/s \quad t_{\text{ox}} \rightarrow t_{\text{ox}}/s \quad N_A \rightarrow sN_A \]
\[ V_{\text{DD}} \rightarrow V_{\text{DD}}/s \quad V_{BS} \rightarrow V_{BS}/s \quad V_T \rightarrow V_T/s \]

We still have \( C_{ox}^* \rightarrow sC_{ox}^* \quad K \rightarrow sK \)

but now we find

\[ \tau \propto \frac{L_{\text{min}}^2 V_{\text{DD}}}{\mu_e [V_{\text{DD}} - V_{Tn}]^2} : \quad \tau \rightarrow \tau/s \]

\[ P_{\text{dyn}} = 3nW_{\text{min}} L_{\text{min}} C_{ox}^* V_{\text{DD}}^2 f : \quad P_{\text{dyn}} \rightarrow P_{\text{dyn}}/s^2 \]

\[ PD_{\text{dyn}} @ f_{\text{max}} = \frac{\mu_e \varepsilon_{ox} V_{\text{DD}} [V_{\text{DD}} - V_{Tn}]^2}{t_{\text{ox}} L_{\text{min}}^2} : \quad PD_{\text{dyn}} @ f_{\text{max}} \rightarrow PD_{\text{dyn}} @ f_{\text{max}} \]

When we scale dimension and voltage we get higher speed and lower power, while holding the power density unchanged.
Scaling Rules, cont. - constant E-field scaling

Threshold voltage:
We've said $V_T$ scales, but this merits some discussion*:

$$V_T(v_{BS}) = V_{FB} + 2\phi_{p-Si} + \frac{t_{ox}}{\varepsilon_{ox}} \sqrt{2\varepsilon_S q N_A \left[2\phi_{p-Si} + |v_{BS}|\right]}$$

Small because with n+-poly Si gate, $\phi_m \approx -\phi_p$ and $V_{FB} \approx -|2\phi_p|$

Dominated by $|v_{BS}|$ if $|v_{BS}| >> |2\phi_p|$

Thus:

$$V_T(v_{BS}) \approx \frac{t_{ox}}{\varepsilon_{ox}} \sqrt{2\varepsilon_S q N_A |v_{BS}|}$$

$$\rightarrow \frac{t_{ox}}{\varepsilon_{ox}} \sqrt{2\varepsilon_S q N_A |v_{BS}|} / |s| \rightarrow V_T / |s|$$

Subthreshold leakage and static power:
Including $v_{BS}$, $I_{D,off}$ is:

$$I_{D,off} = \frac{W}{L} \mu_e V_t^2 \frac{\varepsilon_S q N_A}{2\left[-2\phi_p + |V_{BS}|\right]} e^{-V_T/|nV_t|} \approx \frac{W}{L} \mu_e V_t^2 \frac{\varepsilon_S q N_A}{2 |V_{BS}|} e^{-V_T/|nV_t|}$$

Scaling all the factors, we find that $I_{D,off}$ and $P_{static}$ scale poorly!

$$I_{D,off} \rightarrow s I_{D,off} e^{\left\{(1-1/s)V_T\right\}/nV_t}$$

$$P_{Static} = V_{DD} I_{D,off} \rightarrow P_{Static} e^{\left\{(1-1/s)V_T\right\}/nV_t}$$

* We're talking n-channel here, but similar results are found for the p-channel MOSFETs.
Scaling Rules, cont. - static power scales badly, but...

Static power density's scaling is even worse:

$$PD_{\text{static}} = \frac{I_{D,\text{off}} V_{DD}}{W_{\text{min}} L_{\text{min}}} \rightarrow s \frac{I_{D,\text{off}} e^{(s-1)V_T/snV_t} V_{DD}}{W_{\text{min}} L_{\text{min}}/s^2} \rightarrow s^2 e^{(s-1)V_T/snV_t} PD_{\text{static}}$$

A typical $V_T/nV_t$ is ~10. If $s = \sqrt{2}$, the exponential factor is ~$e^3$, or about 20!

Bottom Line: Static power can no longer be neglected.

Figure source: Intel Web Site
Scaling Rules, cont. - What about velocity saturation?

Do the same constant E-field scaling by 1/s:

\[
\begin{align*}
L_{\text{min}} & \rightarrow L_{\text{min}}/s \\
W & \rightarrow W/s \\
t_{\text{ox}} & \rightarrow t_{\text{ox}}/s \\
N_A & \rightarrow sN_A \\
V_{DD} & \rightarrow V_{DD}/s \\
V_{BS} & \rightarrow V_{BS}/s \\
V_T & \rightarrow V_T/s \\
\end{align*}
\]

\[C_{ox}^* \rightarrow sC_{ox}^* \quad \quad K \rightarrow sK\]

Examining our expressions when velocity saturation is important we find:

\[\tau \propto \frac{L_{\text{min}}V_{DD}}{s_{\text{sat}}[V_{DD} - V_{Tn}]} : \quad \tau \rightarrow \tau/s\]

\[P_{\text{dyn}} = 3nW_{\text{min}}L_{\text{min}}C_{ox}^* V_{DD}^2 f \rightarrow P_{\text{dyn}}/s^2\]

\[PD_{\text{dyn}} @ f_{\text{max}} = \frac{s_{\text{sat}} \varepsilon_{ox} V_{DD}[V_{DD} - V_{Tn}]}{t_{\text{ox}} L_{\text{min}}} \rightarrow PD_{\text{dyn}} @ f_{\text{max}}\]

Amazingly, there is no difference in the scaling behavior of the gate delay, average power, or power density in this case!

Note: Velocity saturation is not a factor in \(I_{D,\text{off}}\)
An historical scaling example - Inside Intel

<table>
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<th>Parameter</th>
<th>386</th>
<th>486</th>
<th>Pentium</th>
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<tr>
<td>Scaling factor, s</td>
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<tr>
<td>$L_{\text{min}}$ (µm)</td>
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<td>$W_n$ (µm)</td>
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<td>$V_T$ (V)</td>
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<td>Fan out</td>
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<td>3</td>
<td>3</td>
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<tr>
<td>$K$ (µA/V²)</td>
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<td>$G_D$ (ps)</td>
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<td>$f_{\text{max}}$ (MHz)</td>
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<td>100</td>
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<tr>
<td>$P_{\text{ave/gate}}$ (mW)</td>
<td>92</td>
<td>23</td>
<td>10</td>
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<tr>
<td>Density</td>
<td>220</td>
<td>880</td>
<td>2,000</td>
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</table>

(kgates/cm² @ 20W/cm² max.)

Sources: Prof. Jesus del Alamo and Intel
An *second look inside Intel* - a slightly different perspective

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<th>Parameter</th>
<th>486</th>
<th>Pentium generations</th>
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<td>$L_{\text{min}}$ (µm)</td>
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<td>SRAM cell area (µm$^2$)</td>
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<tr>
<td>Die size (mm$^2$)</td>
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<td>295</td>
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<tr>
<td>$f_{\text{mzx}}$ (MHz)</td>
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<td>66</td>
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<td>$t_{\text{ox}}$ (nm)</td>
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<td>CMP</td>
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<td>n,p</td>
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<td>Transistors</td>
<td>CMOS</td>
<td>BiCMOS</td>
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Source: Dr. Leon D. Yau, Intel, 10/8/96
Moore's Law - Everything* doubles every 2 years.

* Density, speed, performance, transistors per chip, transistors shipped, transistors per cent, revenues, etc. First stated in 1965 as every year; revised to every 2 years in 1975.
CMOS: the evolution of gate length over 35+ years

Technology Nodes:
A node every 2 yrs
$L_n = 0.7 \ L_{n-1}$
$A_n = 0.5 \ A_{n-1}$
Density doubles every two years.

From the Road Map - more Foil 18

Figures: Prof. D. Antoniadis

MOSFET, $L_g = 0.18 \ \mu m$
(IBM 1999)

Rabies virus
Evolution of Si-MOSFET technology

International Electron Devices Meeting 1.5 Years Ago
Dr. Ghavam Shahidi, IBM Fellow, Dec. 6 at 2009 IEDM:
"..continue to rely on Si to the 11 nm node and beyond [with] fully depleted devices. Companies are just now ramping 32 nm devices into volume production....on track to move to 22 nm node in 2011....15 nm in the 2014-15 timeframe and the 11 nm node in 2017-18. ...scaling to 8 and 5 nm nodes will occur beyond 2020."
"Another common FD device is the FinFET; here, the fin thickness needs to be less than 15nm. The challenges with FinFETs are that it's difficult to obtain good profile control along a vertical wall (especially at a tight pitch) and there's plenty of opportunity for excess parasitic capacitances."

"Along with scaling the depletion width [in conventional device structures], researchers are also looking at scaling the junction depth to be equivalent to the inversion layer thickness, which would eliminate short channel effects."
High Hole Mobility in Strained SiGe-Channel MOSFETs

- change the channel material to SiGe or Ge: increased hole mobility
- hole mobility is 10x higher for strained-Ge-channel p-MOSFETs, compared to standard Si p-MOSFET technology (strained Ge channel can be grown on a Si substrate)
Si Strain Engineering Today

- Many 90-nm technologies are employing some kind of process-induced (“local”) stress to increase current drive
- Enhancements associated with strain-induced mobility improvement and reduction in series resistance (for SiGe S/D)

Recessed SiGe S/D p-MOSFET

T. Ghani, et al., IEDM 2003 (Intel)

Dual-Stress Liner (Si₃N₄)

H.S. Yang, et al., IEDM 2004 (IBM)

Foil courtesy of Prof. Judy Hoyt
**Pushing $f_T$ to 1 THz and beyond:** Even more than in IC scaling, other semiconductors are important if the fastest $f_T$ and highest speed electronics are the goals.
Bipolar Junction Transistors: basic operation and modeling…
… how the base-emitter voltage, $v_{BE}$, controls the collector current, $i_C$
**Heterojunction Bipolar Transistors**: higher mobility materials, graded base to create drift field, different $E_g$ to tailor injection

Work of Prof. Milton Feng and students at University of Illinois
Heterojunction Bipolar Transistors, cont: \( f_T = 685 \, \text{GHz @ R.T.} \)

Notice that performance above 50-100 GHz is extrapolated using the theoretical frequency dependence to get \( f_T \) and \( f_{\text{max}} \) values. This is accepted practice because the instrumentation needed does not exist.
30 nm InAs High-Electron Mobility Transistor
By D. H. Kim and J. A. del Alamo, Funded by Intel and FCSRP-MSD

**Uniqueness:** thin channel containing pure InAs layer to enhance scalability and electron transport ($\mu_e \sim 13,000$ cm$^2$/Vs at 300K)

628 GHz: the highest $f_T$ ever reported on any FET in any material system!
High frequency metrics above 100 GHz: extrapolation to $f_T$, $f_{\text{max}}$

In Dec 2007 at IEDM, Richard Lia and co-workers from Northrup Grumman reported InGaAs HEMTs with $f_{\text{max}}$ between 1.1 and 1.2 THz that they had used to make amplifiers with 15 dB gain at 340 GHz (21 dB at 285 GHz). This is the first report of $f_T$ or $f_{\text{max}} > 1$ THz.

**U**: unilateral gain, $f_{\text{max}}$

**MAG/MSG**: max. available and max stable gain, $f_{\text{max}}$

**H_{21}**: short circuit current gain, $f_T$

Transistor $f_T$'s

Data comparing the $f_T$'s of different types of transistors as a function of their breakdown voltages, which is a reflection of power-handling capability.

Figure courtesy of Professor Rajeev Ram
Ultra-scaled GaN HEMTs

When $L_g = 90$ nm:
$$f_T = 163 \text{ GHz}$$
(demonstrated)

If $L_g = 20$ nm:
$$f_T > 500 \text{ GHz}$$
(in development)

But even higher frequencies could be possible…

If we make $L_g = 20$ nm:
$$\tau_{\text{total}} = \frac{1}{2\pi f_{T,\text{int}}} \sim 120 \text{ fs} < \tau_{\text{scattering}}$$

Ballistic transport expected:
$$v_e \sim 7 \times 10^7 \text{ cm/s} \Rightarrow f_T$$
($v_e > 2 \times 10^8 \text{ cm/s} \text{ in InN}$)

Foil courtesy of Tomas Palacios, UCSB
Gallium Nitride for microelectronic applications

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Unit</th>
<th>Silicon</th>
<th>Gallium arsenide (AlGaAs/InGaAs)</th>
<th>Indium phosphide (InAlAs/InGaAs)</th>
<th>Silicon carbide</th>
<th>Gallium nitride (AlGaN/GaN)</th>
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<td>Electron mobility at 300 K</td>
<td>cm²/Vs</td>
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<td>8500</td>
<td>5400</td>
<td>700</td>
<td>1000–2000</td>
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<tr>
<td>Saturated (peak) electron velocity</td>
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<td>1.0</td>
<td>2.0</td>
<td>1.3</td>
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<tr>
<td>Critical breakdown field</td>
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<td>0.4</td>
<td>0.5</td>
<td>3.0</td>
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Applications of GaN *(Today)*

Wireless Base Stations: RF Power Transistors

Power Conditioning: Mixed-Signal GaN/Si Integration
Automotive Electronics: High Temperature Electronics
Power Transmission Lines: High Voltage Electronics
Flame Sensors: UV Detectors
DVD Information Storage: Blue Laser Diodes
Solid-State White Lighting: Blue/UV LEDs

Wireless: Broadband Access: High Frequency MMICs
Pressure Sensors: MEMS
Heat Sensors: Pyro-Electric Detectors

Nitride-based transistors have many properties that make them very interesting alternative for future microelectronic applications.

Foil courtesy of Tomas Palacios, UCSB
**Mixing technologies and materials on a Si platform:** other routes to keeping performance on the Si roadmap; optoelectronic integration

**Coaxial coupling:**
research at MIT

**Evanescent vertical coupling:**
work at UCSB and Intel

**Grating coupling:**
specific to VCSELs

Source: Dirk Taillaert, INTEC, University of Gent
Solar Cells: Illumination shifts diode curve downward
Electrical power is produced in 4th quadrant

The total current: $i_D(v_{AB}, M) = i_D(v_{AB}, 0) + i_D(0, M)$

$$= I_s\left(e^{qv_{AB}/kT} - 1\right) - AqM(1 - a)$$

Illumination shifts the ideal diode curve down vertically:

Light detection in this quadrant

Power conversion in this quadrant
**Solar Cells:** A single band-gap diode misses much of the solar energy spectrum

Photons with energy, $h\nu$, **less than** $E_g$ are not absorbed, and that part of the spectrum is lost.

Photons with energy, $h\nu$, **more than** $E_g$ are absorbed but all their energy above $E_g$ is lost to the crystal lattice as the electrons and holes "relax" to the bottom of their the lowest energy states. This limits Si solar cell efficiency to $\sim 20\%$.

**The solution:** Stack (layer) several solar cells with differing band-gaps so each optimally absorbs the optimum range of photons.
Solar Cells: Multi-junction solar cells InGaP/GaAs/Ge

Multi-junction cells exceed 50% conversion efficiency. They are costly so are used in sun tracking concentrator systems.
Solar Cells: Multi-junction solar cells InGaP/GaAs/Ge, cont.

The diagram shows the spectral irradiance of sunlight at the top of the atmosphere and radiation at sea level. The graph compares the absorption bands of O$_3$, O$_2$, H$_2$O, and CO$_2$ with the wavelength (nm) range. The solar cells are InGaP, GaAs, Ge, and the lost portion of the spectrum.
High frequency limit of MOSFET operation:

Metric - CS short-circuit current unity gain pt:
$$\omega_T = \frac{g_m}{\left[(C_{gs}+C_{gd})^2 - C_{gd}^2\right]^{1/2}}$$

$$\omega_T$$ is approximately
$$\frac{g_m}{C_{gs}} = \frac{3\mu_e(V_{GS}-V_T)/2L^2}{1/\tau_{ch}}$$

Design lessons: bias at large $$I_D$$; minimize L; use n-channel, not p

High frequency limit of BJT operation:

Metrics - CE short-circuit current gain 3B pt:
$$\omega_\beta = \frac{g_\pi}{(C_\pi + C_\mu)}$$

CE short-circuit current gain unit gain pt:
$$\omega_T = \frac{g_m}{(C_\pi + C_\mu)}$$

$$\omega_T$$ approaches $$1/\tau_b$$ so
$$\omega_T \approx \frac{2D_{min,B}/w_B^2}{2\mu_eV_t/w_B^2} = \frac{1}{\tau_b}$$

Design lessons: bias at high $$I_C$$; minimize $$w_B$$; use npn rather than pnp

The IC Roadmap – Straight silicon nears the end of the road

New structures and new material mixes
Intel opts for FinFETs

Other device research:

III-V Transistors – Digital complements to Si; Microwave ICs
Optoelectronics – LEDs, Laser Diodes, Solar Cells
New Material Families – Organic semiconductors, GaN and friends