Problem 1 - (25 points)

a) [4 pts] A local company has succeeded in making n-type gallium nitride (GaN) in which the hole-electron recombination process in the quasi-neutral regions is very efficient at producing blue light. They want your help designing p-n diodes to take advantage of this material to produce efficient blue light emitting diodes.

i) What type of diodes do you recommend they make, p+-n, p-n, or p-n+, and why?

- p+n (N_Ap >> N_Dn) [ ]
- p-n (N_Ap ≈ N_Dn) [ ]
- p-n+ (N_Ap << N_Dn) [ ]

because

- want lots of excess minority carriers in n-type GaN region
- ⇒ lightly-doped n-region

ii) To optimize the width of n-region, w_n, to get a large fraction of the possible emission without making the layers excessively thick, how large would you recommend they make w_n (compared to the minority carrier diffusion length, L_h), and why?

- w_n = 3 to 4 L_h [ ]
- w_n = L_h [ ]
- w_n = L_h/3, or less [ ]

because

- want w_n >> L_h so they recombine minority carriers

b) [6 pts] So those of you who studied BJTs aren’t disappointed, and so those of you who didn’t should still be able to get some points, here are the only BJT questions on the final. Ten (10) word answers, or less.

i) What is the physical origin of the Early effect in a BJT, and how is it minimized in a well designed device?

Physical origin of the Early effect:
- base width changes w/ V_{CE} (depletion region width changes)
- so minority carrier slope gets steeper
- ⇒ more diffusing current

Design rule to minimize it:
- large base width or collector doping << base doping

ii) Why is an npn BJT preferred over a pnp BJT for high current gain and high speed? [Hint: same reason n-channel is preferred over p-channel MOSFET]

Higher D_{ce} (D_{ce} > D_{np}, M_{c} > M_{p})

iii) What is the meaning of f_T (or ω_T) of a BJT (or any transistor, for that matter), and how does it depend on the base width, w_b?

- Frequency where current gain = 1 (with output shorted)

Meaning:

Dependence on w_b:

\[ w_b \propto \frac{1}{w_b^2} \]

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Problem 1 continued

c) [6 pts] Rank order the following three MOSFET linear amplifier stages in order of increasing output resistance, and give an approximate value for the output resistance if the transistors in each stage are biased in saturation with $V_{BS} = 0$, and so that $g_m = 0.2 \text{ mS}$, and $g_o = g_t = 10 \mu\text{S}$: common-source, common-gate, source follower (common drain). Assume the biasing is done with ideal current sources.

i) Lowest output resistance: Stage ____________

$$R_{out} = \frac{1}{g_m} = \frac{1}{0.2 \text{ mS}} = 5 \text{k} \Omega$$

Approx. Value: 5k Ohms

ii) Intermediate output resistance:

$$R_{out} = \frac{V_o}{I_o} = \frac{1}{g_o} = \frac{1}{10 \mu\text{S}} = 0.1 \text{ M} \Omega \approx 100 \text{k} \Omega$$

Approx. Value: 100k Ohms

iii) Highest output resistance: Stage ____________

$$R_{out} = \frac{g_m}{3g_t} = \frac{0.2 \text{ mS}}{10 \mu\text{S} \times 10 \mu\text{S}} = 20 \text{ M} \Omega$$

Approx. Value: 2 M Ohms

d) [6 pts] The source, drain and substrate of a MOSFET are shorted together and the small signal capacitance of the gate relative to this composite terminal, $C_{gs}$ is measured. It is observed that $C_{gs}$ is constant and equal to $W/LC_{ox}$ when $V_{GS}$ is less than -0.1 V or greater than 0.3 V, but that when $V_{GS}$ is between -0.1 V and 0.3 V $C_{gs}$ is smaller, with the minimum value occurring near -0.1 V.

i) What are the flat-band voltage, $V_{FB}$ and threshold voltage, $V_T$, of this transistor?

$$V_T \text{ where } \frac{m}{3} \text{ capacitance is, } V_T = -0.1 \text{ V}$$

$$V_{FB} = -0.3 \text{ Volts}$$

$$V_T = -0.1 \text{ Volts}$$

ii) What type of MOSFET is this, n-channel or p-channel, and why?

[ ] n-channel [X] p-channel
because negative $V_{GS}$ required to invert channel

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Problem 1 continued

iii) How does \( C_{G} \) in the linear equivalent circuit model of a MOSFET operating in the sub-threshold region compare to \( W L C_{ox}^{*} \)?

- Greater than
- Less than
- Similar to

because no channel charge, less capacitance @ surface (Cap from depletion region)

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e) [3 pts] An isolated n-type silicon sample with \( N_D = 10^{17} \text{ cm}^{-3} \), minority carrier lifetime, \( \tau_{min} \), equal to \( 10^5 \text{ s} \), and perfectly reflecting boundaries (i.e., no surface recombination) has been illuminated for a long time with light generating \( 10^{20} \text{ hole-electron pairs/cm}^2\text{s} \) uniformly throughout its bulk. At \( t = 0 \) the light is extinguished. What is the excess minority carrier density in this sample as a function of time for \( t \geq 0 \)?

\[
\begin{align*}
\text{Uniform optical excitation, uniform doping} & \quad \text{LLL} \quad \text{if } n' = p' \gg n_0 = 10^{17} \text{ cm}^{-3} \\
\text{LLL: } \frac{dp}{dt} + \frac{q}{\tau_{min}} = g(t) \\
p(t = 0) = \frac{10^{15} \text{ cm}^{-3}}{\text{cm}^3} \\
p'(t = 0) = 9 \times 10^{20} \text{ cm}^{-3} \text{s}^{-1} \\
\text{p'(x)} \quad \text{decaying exponential} \\
\end{align*}
\]
Problem 4 - (25 points)

The transistors in the two-stage differential amplifier shown below are all identical with \( V_T = 0.4 \) V, \( C_{ox} = 3 \) pF, \( C_{pd} = 1 \) pF, and \( \lambda = 0 \) V\(^2\), and all are biased so that \( g_m = 6 \) mA/V. The values of the resistances are: \( R_{D1} = R_{D2} = 5 \) k\( \Omega \), and \( R_T = 50 \) k\( \Omega \). The current sources can be considered to be ideal.

![Diagram of the two-stage differential amplifier](image)

a) [4 pts] Calculate the mid-band differential mode voltage gain, \( A_{vd} \), of the amplifier, where \( A_{vd} \) is defined by

\[
A_{vd} = \frac{1}{2} \left( g_m R_{D1} \right) \left( g_m R_{D2} \right) = \frac{1}{2} \left( \frac{6 \text{ mA}}{\text{V}} \right) \left( \frac{5 \text{ k}\Omega}{1} \right) = 30
\]

\[
A_{vd} = 45.0
\]

b) [3 pts] What is the mid-band common mode voltage gain, \( A_{vc} \), of this amplifier, where \( A_{vc} \) is defined by

\[
A_{vc} = \frac{g_m R_D}{1 + g_m (2 V_{os} \cdot \text{cm})} \approx \infty
\]

\[
A_{vc} = 0
\]

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Problem 4 continued

c) [4 pts] If $V_+ = 1.5\, \text{V}$, $V_- = -1.5\, \text{V}$, and $I_{\text{BIAS}} = 0.2\, \text{mA}$, and if the transistors are all biased with $(V_{\text{CE}} - V_{T}) = 0.2\, \text{V}$, what is the **maximum** common-mode input voltage for this amplifier?

\[
V_D = V^+ - \left(\frac{I_{\text{BIAS}}}{2}\right) R_D = 0.5\, \text{V}
\]

\[
V_D = 1.5\, \text{V} - \left(0.1\, \text{mA}\right) (5\, \text{k}\Omega)
\]

\[
V_D = 1.0\, \text{V} \rightarrow \text{Fixed}
\]

\[
V_{\text{IC,max}} = 0.8\, \text{V} \rightarrow V_{\text{IC,max}} = 0.8\, \text{V} + \frac{0.6\, \text{V}}{V_{\text{IC}}} = \boxed{1.4}\, \text{Volts}
\]

d) [3 pts] Calculate the quiescent power dissipation in this amplifier, $P_{Q}$, under the bias conditions specified in Part c?

\[
P_Q = \frac{(3\, \text{V})(0.4\, \text{mA})}{\text{Watts}} = 1.2\, \text{mW}
\]

e) [3 pts] What value of $R_{D2}$ would make the quiescent output voltage, $V_{\text{OUT}}$, zero? (Note: Do not change $R_{D2}$ to this value in the remaining parts of this question; it should stay $5\, \text{k}\Omega$).

\[
V_{\text{OUT}} = 1.5\, \text{V} - \left(\frac{I_{\text{BIAS}}}{2}\right) R_{D2} = 0\, \text{V}
\]

\[
R_{D2} = \frac{1.5\, \text{V}}{0.1\, \text{mA}} = 15\, \text{k}\Omega
\]

\[
R_{D2} = \boxed{15\, \text{k}\Omega}
\] Ohms

f) [4 pts] Calculate the bandwidth, $\omega_{\text{HI}}$, of the amplifier in differential mode. Assume $C_{\text{td}}$ is negligible, and use the Miller effect to combine $C_{\text{gs}}$ and $C_{\text{pd}}$ at the input to each stage, before you calculate the open circuit time constants to estimate $\omega_{\text{HI}}$.

\[
\tau_{\text{Hant}} = \left(R_{\text{T}}\right) \left(C_{\text{gs}} + C_{\text{sd}} \left(1 + \frac{g_m R_{\text{D}}}{g_{\text{m}}}\right)\right) = 1.7\, \mu\text{s}
\]

\[
\omega_{\text{HI}} = \frac{1}{\tau_{\text{Hant}}} = \frac{1}{1.7\, \mu\text{s}} = 588\, \text{rad/s}
\]

\[
\tau_{\text{Mid}} = \left(R_{\text{D}}\right) \left(34\, \text{pF} + C_{\text{sd}} \left(1 + \frac{g_m R_{\text{D}}}{g_{\text{m}}}\right)\right) = 0.175\, \mu\text{s}
\]

\[
\tau_{\text{Out}} = \left(R_{\text{D}}\right) \left(1\, \text{pF}\right) = 0.005\, \mu\text{s}
\]

\[
\omega_{\text{HI}} = \frac{1}{\tau_{\text{Out}}} = \frac{1}{0.005\, \mu\text{s}} = 200\, \text{kHz}
\]

$\omega_{\text{HI}} = \boxed{532 \times 10^3}\, \text{s}^{-1}$

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$f_{\text{HI}} = 85\, \text{kHz}$
g) [4 pts] To increase the bandwidth of the circuit, we add a third amplifier stage (a preamplifier) to each input as shown in the figure below. The transconductance of the two new transistors is also $g_m = 6 \, \text{mS}$.

In the space below, explain in 25 words or less why the bandwidth is increased by this change. You can assume that the open circuit time constants associated with the intrinsic capacitances of the preamplifier transistors do not contribute to $\omega_{HI}$.

Source follower has low output resistance, so time constant smaller, higher BW

$R_{out} = \frac{1}{g_m} = 167 \, \Omega \ll 50 \, \text{k}\Omega = R_T$

300x difference

End of Problem 4; end of Final Exam. Have a great summer.